# Scheme of Teaching and Examination

**M.Tech. (DIGITAL ELECTRONICS ) in the Department of Electronics & Telecommunication**

## III SEMESTER

<table>
<thead>
<tr>
<th>S.No</th>
<th>Board of Study</th>
<th>Subject Code</th>
<th>Subject Name</th>
<th>Periods per week</th>
<th>Scheme of Exam</th>
<th>Total Marks</th>
<th>Credit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>T</td>
<td>P</td>
<td>Theory/Practical</td>
</tr>
<tr>
<td></td>
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<td>L</td>
<td>T</td>
<td>P</td>
<td>ESE</td>
</tr>
<tr>
<td>1</td>
<td>Electronics &amp; Telecom</td>
<td>555311 (28)</td>
<td>Digital Coding Techniques</td>
<td>3</td>
<td>1</td>
<td>-</td>
<td>100</td>
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<td>2</td>
<td>Refer Table – III</td>
<td></td>
<td>Elective –III</td>
<td>3</td>
<td>1</td>
<td>-</td>
<td>100</td>
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<tr>
<td>3</td>
<td>Electronics &amp; Telecom</td>
<td>555321 (28)</td>
<td>Preliminary Project</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>100</td>
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<tr>
<td>4</td>
<td>Electronics &amp; Telecom</td>
<td>555322 (28)</td>
<td>Seminar based on Dissertation</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>-</td>
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<td>6</td>
<td>2</td>
<td>18</td>
<td>300</td>
</tr>
</tbody>
</table>

L-Lecture, T- Tutorial, P- Practical, ESE- End Semester Examination, CT- Class Test, TA- Teacher’s Assessment

### Table – III

#### Elective – III

<table>
<thead>
<tr>
<th>Board of Study</th>
<th>Code</th>
<th>Subject</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronics &amp; Telecom</td>
<td>555331 (28)</td>
<td>Network Modulling</td>
</tr>
<tr>
<td>Electronics &amp; Telecom</td>
<td>555332 (28)</td>
<td>Neural Network and Application</td>
</tr>
<tr>
<td>Electronics &amp; Telecom</td>
<td>555333 (28)</td>
<td>ASIC Design</td>
</tr>
<tr>
<td>Electronics &amp; Telecom</td>
<td>555334 (28)</td>
<td>Digital Switching Systems</td>
</tr>
</tbody>
</table>

**Note (1)** - 1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a particular academic session.

**Note (2)** - Choice of elective course once made for an examination cannot be changed in future examinations.
UNIT – I

UNIT – II

UNIT – III
Coding Schemes: Cyclic codes, method for generating cyclic: codes, matrix description of cyclic codes, Burst error correction, Fire codes, CRC codes, Convolution codes. Tree codes and trellis Codes, analytical representation, decoding Convolution codes.

UNIT – IV
Cryptographic techniques: Introduction to cryptography; cryptographic protocols, hash function, key management. communication using public key cryptography, secret key algorithm, digital signatures, keys management, encryption algorithms, Block Cipher, Transposition Cipher. Multiple encryption, stream cipher, RSA algorithm, data encryption standard, cryptanalysis.

UNIT – V

Text Books:
- Ranjan Bose, Fundamentals of Information Theory, Coding and Cryptography
- R.B. Wells, Applied Coding & Information Theory for Engineers, Prentice-Hall
- Khalid Sayood, Introduction to Data Compression

Reference Books:
A. Burr, Modulation & coding for wireless communications Prentice-Hall
- J.G. Proakis & M. Salehi, Communication systems engineering Prentice-Hall
- Shu Lin & D.J. Costello, Jr. Error control coding Prentice-Hall
- S. Haykin & M. Moher, Modern wireless communications Prentice-Hall
- Nelson M, The Data Compression Book
UNIT - I
SYSTEM MODELS AND ROLE OF SIMULATION: Basic concepts and nomenclature, Types of system- Deterministic, stochastic, continuous and discrete systems, System simulation-Uses of simulation and its limitations, Steps in simulation studies.

UNIT - II
STATISTICAL TOOLS: Generation and testing of pseudorandom numbers, Random variety generation for Uniform, Exponential, Normal and Poisson distributions, Sampling and Estimation (Maximum likelihood estimation, Confidence interval estimation), Discrete Event Simulation : Representation of time, Approaches to discrete event simulation, Queuing models-Single and multiserver queues, Steady state behaviors of queues, Network of queues, Inventory system simulation, Programming languages for discrete event system simulation-GPSS, SIMSCRIPT (Brief Overview).

UNIT - III
MODELING AND PERFORMANCE EVALUATION OF COMPUTER SYSTEMS: Behavioral, Data flow and structural modeling, Overview of Hardware Modeling and Simulation using VHDL, VHDL Description for design reuse, test generation and fault simulation for behavioral model. Single service center models, Central server models, models of interactive systems, use of VHDL in front-end and back-end system development. Evaluation of multiprocessor systems, workload characterization & Benchmarks.

UNIT-IV
CONTINUOUS SYSTEM SIMULATION: Continuous system models-Open and closed loop systems, Models described by differential equations, Systems dynamics (Growth and decay models, Systems dynamics diagram), Simulations of aircraft models, Biological and sociological systems simulation, Simulation languages overview-CSMP.

UNIT-V
VIRTUAL REALITY MODELING: Overview of virtual reality modeling language VRML 2.0, Creating dynamic worlds, Integrating JavaScript’s with VRML, Verification and Validation of Simulation Models : Goals of model verification and validation, Input data analysis, Output analysis, Sensitivity analysis, Hypothesis testing, Performance measures and their estimation.

Text Books:

Reference Books:
CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. III Sem.**  
Subject: **Neural Network and Applications**  
Branch: **Electronic & Telecom.**  
Code: **555332 (28)**  
Total Theory Periods: **40**  
Total Tutorial Periods: **12**  
Total Marks in end Semester Exam.: **100**  
Minimum number of class tests to be conducted: **02.**

UNIT - I  
Biological, Analogy, Architecture classification, Neural Models, Learning Paradigm and Rule, single unit mapping and the perception.

UNIT – II  

UNIT - III  
PCA, SOM, LVQ, Hopfield Networks, Associative Memories, RBF Networks, Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

UNIT – IV  

UNIT – V  

Text Books:

Reference Books:
5. Artificial Neural Networks, B. Yegnanarayana, PHI.
CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Subject: ASIC Design  Code: 555333 (28)
Total Theory Periods: 40  Total Tutorial Periods: 12

Total Marks in end Semester Exam.: 100
Minimum number of class tests to be conducted: 02.

UNIT – I
Introduction to ASICs: - Types of ASICs - Design flow - CMOS logic: CMOS transistors CMOS Design rules - Combinational Logic Cell -Sequential logic cell - Data path logic cell I/O cells - ASIC library design: Transistors as Resistors - Transistor Parasitic Capacitance-Logical effort.

UNIT – II

UNIT – III

UNIT – IV

UNIT – V
ASIC construction: System partition - FPGA partitioning - partitioning methods - Floor planning and placement: floor planning - placement - physical design flow. Routing : global routing - detailed routing - special routing - circuit extraction - DRC.

Text book:

Reference Books:
UNIT – I
Digital Switching Systems (DSS) fundamentals: Introduction, digital switching system, hierarchy and evolution of switching systems. Major digital switching systems (Lucent 5ESS switching system, Nortel’s DMS 100, Ericsson’s AXE 10, etc.,)

UNIT – II
Communications and control: Introduction, switching communication and control, functions of interface controller, network control processor, central processor, control architectures, switches fabric.

UNIT – III
Reliability modeling and analysis: Introduction, downtimes in DSS, reliability assessment techniques, failure models, state transition diagrams for central processor community, clock sub-system, network controller sub-system, switching network.

UNIT – IV
Switching System Software (SSS) and quality analysis: Basic software architecture, call models, call features, life cycle of SSS software development, methodology of accessing quality of SSS to CMM and ISO models.

UNIT – V

Text Books:

Reference Books