Chhattisgarh Swami Vivekanand Technical University, Bhilai

Scheme of Teaching and Examination

M.Tech. (Computer Technology)

Semester - I

S.N.	Board of Study	Subject Code	Subject Name	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
							Theory/Practical				
				L	T	P	ESE	CT	TA		
1	Computer Sc. & Engg.	554111(22)	Compiler Design	3	1	-	100	20	20	140	4
2	Computer Sc. & Engg.	522112(22)	Java Programming & Applications	3	1	-	100	20	20	140	4
3	Computer Sc. & Engg.	522113(22)	Advanced Computer Architecture	3	1	-	100	20	20	140	4
4	Computer Sc. & Engg.	554112(22)	Advanced Computer Communication Network	3	1	-	100	20	20	140	4
5	Computer Sc. & Engg.	Elective –I		3	1	-	100	20	20	140	4
6	Computer Sc. & Engg.	554121(22)	Compiler Design Lab	-	-	3	75		75	150	2
7	Computer Sc. & Engg.	554122(22)	Java Programming & Applications Lab	-	-	3	75		75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

L-Lecture, T- Tutorial, P - Practical, ESE- End Semester Examination, CT- Class Test, TA- Teacher's Assessment
Note : Duration of all theory papers will be of Three Hours.

Elective –I			
S.N.	**Board of Study**	**Code**	**Subject Name**
1	Computer Science & Engineering	**522133(22)**	System Simulation
2	Computer Science & Engineering	**522134(22)**	Analysis and Design of Algorithms
3	Computer Science & Engineering	**522135(22)**	Digital Signal Processing

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology.**
Subject: Compiler Design **Code: 554111 (22)**
Total Theory Periods: 40 **Total Tut Periods: 12**
Total Marks in end Semester Exam: 100
Minimum Number of Class Tests to be conducted: 02

Unit - I

Introduction

Compilers – Analysis of the source program, Phases of a compiler, Cousins of the Compiler, Grouping of Phases, Compiler construction tools; Lexical Analysis – Role of Lexical Analyzer, Input Buffering, Specification of Tokens. Lexical phase errors, syntactic phase errors, semantic phase errors.

Unit – II

Syntax Analysis and Parsing Techniques

Role of the parser, Writing Grammars –Context-Free Grammars, Top Down parsing, Recursive Descent Parsing, Predictive Parsing, Bottom-up parsing, Shift Reduce Parsing, Operator Precedent Parsing, LR Parsers, SLR Parser, Canonical LR Parser, LALR Parser.

Unit - III

Intermediate Code Generation & Syntax Directed Translation

Intermediate languages, Declarations, Assignment Statements, Boolean Expressions – Case Statements, Back patching, Procedure calls, Syntax Directed Translation Scheme-Implementation of Syntax Directed Translators-Intermediate code Postfix Notation, Parse trees and syntax trees, Trees three address code, Quadruples, Triples, Translation of Assignment statements, Boolean expressions-Declaration, Flow control statements, Back-patching.

Unit - IV

Code Generation

Issues in the design of code generator, Target Machine, Runtime Storage Management, Basic Blocks and Flow Graphs, Next-Use Information, A Simple Code Generator, DAG Representation of Basic Blocks, Peephole Optimization.

Unit - V

Code Optimization and Run Time Environments

Introduction– Principal Sources of Optimization, Optimization of basic Blocks, Introduction to Global Data Flow Analysis, Runtime Environments, Source Language issues, Storage Organization, Storage Allocation strategies, Access to non-local names, Parameter Passing.

Text Books

1. Alfred Aho, Ravi Sethi, and Jeffrey D Ullman, “Compilers Principles, Techniques and Tools”, Pearson Education Asia.

References Books

1. J.P. Bennet, “Introduction to Compiler Techniques”, Second Edition, Tata McGraw-Hill, 2003.
2. Henk Alblas and Albert Nymeyer, “Practice and Principles of Compiler Building with C”, PHI, 2001.
3. Kenneth C. Louden, “Compiler Construction: Principles and Practice”, Thompson Learning.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**

Subject: Java Programming and Applications **Code: 522112(22)**
Total Theory Periods: 40 **Total Tut. Periods: 12**
Total Marks in End Semester Exam: 100
Minimum Number of Class Tests to be conducted: 02

Unit-I

Introduction to Java

Importance and Features of Java, Concepts of Java Virtual machine (JVM), Keywords, Constants, Variables and Data types, Operators and Expressions, Control Statements, Conditional Statements, Loops and Iterations. Class Definition, Adding Variables and Methods, Creating Objects, Constructors, Defining methods, Calling methods, Method overloading. Creating an Array, One and Two Dimensional Array, String Array and Methods String and String Buffer classes, Wrapper Classes.

Unit-II

Inheritance

Basic Types, Super classes, Multilevel Hierarchy Abstract and Final classes, Object Class, Packages and Interfaces, Access protection, extending Interfaces, Exception Handling, Fundamental Exception types, Uncaught Exception, Throw, Throws, final Methods, Creating own Exceptions

Unit-III

Multithreaded programming

Review of Fundamentals, Java Thread Model, Synchronization, Messaging, Thread Class, Runable Interface, Inter Thread Communication, Monitors, Deadlock, Producer/ Consumer Problems, Wait() and notify(), Performance Issues.

Unit-IV

Input/output

Basics, Streams, Byte and Character Streams, Predefined Streams, Reading and Writing from Console and Files, using Java Packages.

Networking in Java

Networking fundamentals, Client/server model, Internet addresses, Sockets, networking classes and Interfaces, using Java.net Package, TCP/IP and Datagram Programming, HTTP Protocol and URLs.

Unit-V

Event Handling

Different Mechanism, the Delegation Event Model, Classes, Event Listener Interfaces, Adapter and Inner Classes, Working with Windows, Graphics and Text, using AWT Controls, Layout Managers and Menus, Handling Image, Animation, Sound and Video Java Applet, Introduction to Swings, JDBC and Servlets.

Programming Graphical System:

Text Books

1. Herbert Schildt, “The Complete Reference Java 2”, Tata McGraw Hill.
2. Khlid A. Mughal and R.W. Rasmussen, “A Programmer Guide to Java”, Addison Wesley.

3. Ivan Bayross, “Web Enabled Commercial Application Java 2” - B.P.B. Publication

Reference Books

1. Cay S. Horstmann and Gary Cornell, “Core Java(TM), Volume I and II”, Prentice Hall, Sun Microsystems Press.
2. Patrick Niemeyer and Josh Peck, “Exploring Java”, O'Reilly Media.
3. Richard M Haefel and Bill Burke, “Enterprise Java Beans 3.0”, O'Reilly Media.
4. George Reese, “Database Programming with JDBC and Java”, O'Reilly Media
5. Michael Wooldridge, “An Introduction to Multi Agent Systems”, John Wiley & Sons.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**
Subject: Advanced Computer Architecture **Code: 522113(22)**
Total Theory Periods: 40 **Total Tut. Periods: 12**
Total Marks in End Semester Exam: 100
Minimum number of Class Tests to be conducted: 02

Unit -I

The state of computing, Multiprocessors and Multi Computers, Multi-Vector and SIMD Computers. Conditions of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures, Network properties and Routing, Static Interconnection Networks and Dynamic Interconnection Networks, MPI and PVM Architecture.

UNIT - II

Advanced Processor Technology- CISC, RISC, Superscalar, Vector, VLIW and Symbolic Processors, Memory Hierarchy Technology, Virtual Memory Technology (Virtual memory Models, TLB, Paging and Segmentation).

UNIT - III

Cache Memory Organization, Shared Memory Organization, Sequential and Weak Consistency Models

UNIT - IV

Linear Pipeline Processors, Nonlinear Pipeline processors, Instruction Pipeline Design, Arithmetic Pipeline Design

UNIT - V

Multiprocessors System Interconnects, Cache Coherence and Synchronization Mechanisms, Vector Processing Principles, Multi-vector Multiprocessors and Data Flow Architecture.

Text Book

1. Kai Hwang "Advanced Computer Architecture", McGraw Hill.

Reference Books

1. W. Stallings, "Computer Organization and Architecture", Prentice Hall Inc.
2. V. Rajaraman and C. Siva Ram Murthy, "Parallel Computers: Architecture and Programming", Prentice Hall of India Pvt. Ltd.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**
Subject: Advanced Computer Communication Network **Code: 554112 (22)**
Total Theory Periods: 40 **Total Tut. Periods: 12**
Total Marks in End Semester Exam: 100
Minimum number of class tests to be conducted: 02

Unit -I

Introduction

Data Communications – Characteristics, Components – Protocols and Standards Networking – Data transmission Concepts and Terminology – Transmission Media – Reference models – OSI, TCP/IP – Wired LAN – categories of standard Ethernet, Fast Ethernet, Gigabit Ethernet, Token ring, FDDI – Bridge operation – Functions of Bridge, Bridge protocol architecture, Source Routing, Route Discovery and maintenance.

Unit- II

Data Communications

Transmission Impairments – Attenuation, Delay distortion, Noise – Channel Capacity – Concepts, Nyquist and Shannon's Theorems for maximum data rate of a channel – Data link Control – Flow Control, Error Detection and Correction – Error Correcting Codes, Hamming code – Polynomial code checksum, HDLC - Multiplexing – Frequency Division Multiplexing, Time division multiplexing, Wavelength Division Multiplexing.

Unit -III

Network Layer

Design issues – Routing Algorithms – Optimality Principle, Shortest Path Routing, Flooding, Broadcast Routing, Routing for Mobile Hosts, Routing in Ad Hoc Networks – Congestion Control Algorithms – General Principles, Preventive Policies, Virtual Circuit Subnets, Jitter Control – Quality of service – Requirements, Techniques for Achieving Good Quality of Service – Internetworking – IP Address, Mobile IP, IPV6.

UNIT IV

TRANSPORT LAYER

Transport layer – Transport Service Primitives, Elements of Transport Protocols – Addressing, Connection Establishment, Connection Release, Flow Control and Buffering, Multiplexing, Crash Recovery – Example as a Finite State Machine – Internet transport protocols – UDP, RPC, RTP – TCP protocol, TCP Connection Establishment, Connection Release, TCP Transmission Policy, TCP Congestion Control.

UNIT V

APPLICATION LAYER

Message formats – RFC822, MIME, SMTP, POP3 -DNS – Cookies – WAP – Network Security – Symmetric-key Algorithms - DES, AES – Public-Key Algorithms – RSA, Digital signatures – Symmetric-key, Public-key, MD5, SHA-1 – Diffie-Hellman Key Exchange – SSL.

Text Books

1. Andrew S Tenenbaum "Computer Networks", PHI, Fourth Edition, 2003.
2. Fehrouz A Foruzan "Data Communication and Networking", TMH, 2004.

Reference Book

1. William Stallings, "Data and Computer Communications", Fifth Edition, PHI, 2001.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**

Subject: System Simulation **Code: 522133(22)**

Total Theory Periods: 40 **Total Tut. Periods: 12**

Total Marks in End Semester Exam: 100

Minimum number of class tests to be conducted: 02

Unit - I

System Models: The Concept of a System, System Environment, Stochastic Activities, Continuous and Discrete Systems, System Modeling, Types of Models, Principles used in Modeling.

System Studies: Subsystems, a Corporate Model, Types of System Study, System Analysis, System Design, System Postulation.

System Simulation: The Technique of Simulation, The Monte Carlo Method, Comparison of Simulation and Analytical Methods, Types of System Simulation, Numerical Computation Technique of Continuous Models, Numerical Computation Techniques for Discrete Models, Distributed Lag Models, Cobweb Models, The Process of Simulation.

Unit-II

Continuous System Simulation: Continuous System Models, Differential Equations, Analog Computers, Analog Methods, Hybrid Computers, CSMP III, Hybrid Simulation, Feedback Systems, Simulation of an Autopilot.

System Dynamics: Exponential Growth Models, Exponential Decay Models, Logistic Curves,

Generalization of Growth Models, System Dynamics Diagrams, Multi Segment Models, Feedback in Socio-Economic Systems, a Biological Example, World Models, the Dynamo Language.

Probability concepts in Simulation: Stochastic variables, Discrete and Continuous Probability Functions, Numerical Evaluation, Random Number Generators, Discrete Distribution Generation.

Unit-III

Introduction To GPSS: GPSS Programs, General Description, Action Times, Succession of Events, Choice of Paths, Simulation of a Manufacturing Shop, Facilities and Storages, Gathering Statistics, Conditional Transfers, Program Control Statements.

GPSS Examples: Priorities and Parameters, SNAs, Functions, Simulation of a Super Market, Transfer Modes, Logic Switches, Testing Conditions, GPSS Model of a Simple Telephone System, Set Operations.

Unit-IV

The Basic Nature of Simulation, When to Simulate? Simulation of a Single Server Queue, Simulation of a Two Server Queue, Simulation of a More General Queue, Simulation of a PERT Network.

Unit-V

Simulation of a General Inventory System, Simulation of an Inventory Policy (P, Q), Simulation of an Inventory System with Buffer Stock, Simulation Languages.

Text Books

1. Geoffrey Gordon, “System simulation”, Prentice Hall of India.
2. Narsingh Deo, “System Simulation with Digital Computer”, Prentice Hall of India (EEE)
3. Frank L. Severance, “System Modeling & Simulation: An Introduction”, John Wiley & Sons, 2001.

Reference Books

1. Averill M. Law, “Simulation Modeling and Analysis”, McGraw Hill.
2. J. Banks, “Discrete Event System Simulation”, Atlantic Publications.
3. F. Cellier and E. Kofman, “Continuous System Simulation”, Springer Verlog.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**
Subject: Analysis and Design of Algorithms **Code: 522134(22)**
Total Theory Periods: 40 **Total Tut. Periods: 12**
Total Marks in end Semester Exam: 100
Minimum number of class tests to be conducted: 02

Unit -I

Algorithm Development for Problem Solving, Analyzing Efficiency of Algorithm, Asymptotic Growth Rates. ADT Specification and Design Techniques, Elementary ADTs-Lists Trees, Stacks and Queues. Recursion and Induction Recursive procedures, Induction Proofs, Proving Correctness, Recurrence Relations, Recursion Trees.

Unit -II

Divide and Conquer technique of problem solving, sorting algorithms: Quicksort, Merge Sort, Merging Sorted sequences, Lower brands for sorting, heap sort, shell sort, radix sort, Dynamic sets and searching : Array doubling, Red Black trees, hashing high, priority queues.

Unit -III

Graphs: Definitions and representations, traversal, DFS and BFS., DFS on undirected graphs.

Greedy Algorithms: Prim's Algorithm, Single Source Shortest Paths, Kruskal's Minimal Spanning Trees. Transitive closure, APSP problem, Computing Transitive Closure for Matrix Operations.

Unit- IV

Dynamic Programming: Sub problem, Graphs and their Traversal, Multiplying a Sequence of matrices, Optimal Binary Search Tree Construction.

Unit-V

String Matching: Knuth - Moore-Pratt Algorithm, Boyer- Moore Algorithm, P & N P, NP Complete Algorithms.

Text Book :

1. Sara Baase, Allean Van Gelder: "Computer Algorithms, Introduction to Design and Analysis, 3rd Edition, Pearson Education, Asia.
2. "The Design and Analysis of Computer Algorithms" by AHO/ULLMAN/HOPCROFT

References :

1. Corman, Leiserson & Rivest : Introduction to Algorithms, PHI publication.
2. Aho, "Data Structures and Algorithms", Pearson Education.
3. Aho, "Design & Analysis of Computer Algorithms", Pearson Education.
4. Donald E. Knuth : "The Art of Computer Programming (Vol I to III), Pearson Education.
5. Mark Allen Weiss "Data Structures and Algorithm Analysis in C", second edition, Pearson Education.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**

Subject: Digital Signal Processing **Code: 522135(22)**
Total Theory Periods: 40 **Total Tut. Periods: 12**
Total Marks in End Semester Exam: 100
Minimum number of class tests to be conducted: 02

Unit-I

Discrete Signals and Systems: Basic elements of DSP, Classification of discrete time signals, signal representation, Operation on DTS, Classification of Discrete Time Systems (DTS), Representation of Arbitrary Sequence, Impulse Response and Convolution Sum, Solution of Difference Equation Using Direct Method, FIR and IIR Systems, Stable and Unstable Systems. Frequency Response, Transfer Function, Correlation and Auto Correlation. The Z- Transforms: Z- Transform and ROC of Finite and Infinite Duration Sequence, Stability and ROC, Properties of ZT, Inverse Z-Transforms (IZT), solution of differential equation using ZT, analysis of LTI system.

Unit - II

Frequency domain representation of Discrete signals: Discrete time Fourier transform (DTFT), Inverse DTFT, Properties of DTFT, Discrete Fourier Transform (DFT), Properties of DFT, IDFT, Twiddle Factor, DFT & IDFT using Matrix Method, Circular Convolution, Analytical, Graphical and Matrix method for circular convolution, Fast convolution, Fast Fourier transform (FFT), Radix – 2 FFT, DIT-FFT, DIT-IFFT, DIF-FFT, Radix –2 DIF – IFFT, Composite radix FFT, Applications of FFT.

Unit - III

Implementation of discrete-time systems: Block diagram and signal flow graph representation of IIR and FIR filters, Realization of IIR filters Direct –I, Direct-II, Cascade, Parallel, Ladder and Transposed Realization), Realization of FIR filters (Direct, Cascade and linear phase FIR structure). Design of Digital Filter, Specification of FIR Filters, General Consideration, Design of FIR Filters, Symmetric and Anti-symmetric FIR Filter, Design of FIR Filter using Windows, Frequency Sampling Method, Hilbert Transformers.

Unit - IV

Filter Design Technique: Design of DTIIR filters. From continuous time filters, Introduction to analog filters for designing Digital filters (Butter Worth and Chebyshev Filters), filters design using Impulse Invariant, Bilinear Z Transform, Matched Z-Transform and Approximation of Derivatives Methods, Frequency Transformation, Frequency Transformations, Design of IIR Filters in Frequency Domain, Difference between FIR and IIR filters.

Unit - V

Real Time DSP Systems: Real time DSP systems: DSP and Its Benefits, Key DSP Operations, Typical Real time DSP System, ADC Process, Uniform and Non-uniform Quantization and Encoding DAC Process, Signal Recovery, Sampling of Low Pass and Band Pass Signals, Digital Signal Processors, Evaluation Boards for Real Time Signal Processing, TMS320C10 Forget Board, DSP application, Adaptive removal of ocular artifacts from human EEGs: Multirate Digital Signal Processing, Decimation by Factor D, Interpolation by Factor I, Filter and Implementation for Sampling Rate Conversion, Multistage Implementation of Sampling Rate Conversion, Sampling Rate Conversion of Band Pass Signals, Application of Multirate Signal Processing.

Text Books

1. Proakis J.G. and D.G. Manolakis, “Digital Signal Processing”, Prentice Hall of India.
2. Ifeachor Emmanuel C. and Barrie W. Jervis, “Digital Signal Processing: A Practical Approach” Pearson Education Ltd., Fifth Indian Reprint, 2005.

Reference Books

1. Jonsson Jonny, “Digital Signal Processing”, Tata McGraw Hill Publication.
2. Schafer R.W. and A.V. Oppehbein, “Digital Signal Processing”, Prentice Hall of India.
3. Kue R., “Introduction to Digital Signal Processing”, McGraw Hill.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**
Subject: Compiler Design Lab **Code: 554121 (22)**
Total Practical Periods: 40
Total Marks in End Sem. Exam: 75

Experiments to be performed

1. WAP to generate tokens in give source language using in C.
2. Extend program 1 to check whether a given token is a key word or a data type. If it is data type check whether it is valid data type.
3. Extend program 2 to implement a lexical analyzer in C.
4. Use LEX tool to implement a lexical analyzer.
5. Develop an operator precedence a parser (construct a parse table algo)/ LL(1) parser.
6. Implement a recursive descent parser for an expression grammar that generates arithmetic expressions with digits, + and *.
7. Use YACC and LEX to implement a parser for the same grammar as given in problem
8. Write semantic rules to the YACC program in problem 5 and implement a calculator that takes an expression with digits, + and * and computes and prints its value.
9. Implement the front end of a compiler that generates the three address code for a simple language with: one data type integer, arithmetic operators, relational operators, variable declaration statement, one conditional construct, one iterative construct and assignment statement.
10. Implement the back end of the compiler which takes the three address code generated in problems 7 and 8, and produces the 8086 assembly language instructions that can be assembled and run using an 8086 assembler. The target assemblies instructions can be simple move, add, sub, and jump. Also simple addressing modes are used.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: M. Tech. I Sem. **Branch: Computer Technology**
Subject: Java Programming Lab **Code: 554112(22)**
Total Practical Periods : 40
Total Marks in End Sem. Exam: 75

Experiments to be performed

1. Write a program for matrix multiplication. Use InputStream Reader and Buffered Reader classes for Input/Output.
2. Write a program to create a user defined Exception when the user inputs the marks which exceed more than 100.
3. Write a program to animate a string on Applet. Use the concept of Multithreading.
4. Write a program to design a calculator using the AWT controls provided in Java.
5. Write a program for Client Server communication using either UDP or TCP protocols. Use Server Socket and Socket classes.
6. Write a program to create some of the features of Notepad. Use Swings for designing this application.
7. Create functions like multiply, addition and subtraction respectively. Invoke these functions from remote system by using the concept of Remote Method Invocation in Java.
8. Create a form containing fields name and password respectively, using applet as a container
9. The input entered in these fields should be stored in the database .Use JDBC connectivity for implementing this program.
10. Write a program to create a small portal which contains the registration form of students. Use JDBC.
11. Write a program create a bean component in Java for addition of two numbers.