Chhattisgarh Swami Vivekanand Technical University, Bhilai

SCHEME OF MASTER OF TECHNOLOGY

Electronics & Telecommunication Engineering (VLSI & Embedded System Design)

M. Tech. [Fourth Semester]

Sr. No.	Board Of Studies	Code	Subject	Weekly Teaching hours			Scheme of Examination			Grand Total	Credits
				L	T	P	ESE	CT	TA		
1	**Electronics & Telecom**	572421 (28)	Dissertation	6	--	34	300	--	200	500	23
Total				**6**	**--**	**34**	**300**	**--**	**200**	**500**	**23**

L – Lecture, T – Tutorial, P – Practical, ESE- End Semester Exam , CT- Class Test TA – Teacher's Assessment