Chhattisgarh Swami Vivekanand Technical University, Bhilai

SCHEME OF MASTER OF TECHNOLOGY

Electronics & Telecommunication Engineering (VLSI & Embedded System Design)

M. Tech. [Second Semester]

Sr. No.	Board Of Studies	Code	Subject	Weekly Teaching hours			Scheme of Examination			Grand Total	Credits
				L	T	P	ESE	CT	TA		
1	E&Tc	572211 (28)	Mixed Signal and RF Circuit Design	3	1	--	100	20	20	140	4
2	E&Tc	572212 (28)	CMOS Digital Circuit Design	3	1	--	100	20	20	140	4
3	E&Tc	572213 (28)	Digital Signal Processor	3	1	--	100	20	20	140	4
4	E&Tc	572214 (28)	Application Specific Integrated Circuits	3	1	--	100	20	20	140	4
5	E&Tc	**Reference Table -I**		3	1	--	100	20	20	140	4
6	E&Tc	572221 (28)	Lab-I CMOS Circuit Design	--	--	3	75		75	150	2
7	E&Tc	572222(28)	Lab-II DSP Processor	--	--	3	75		75	150	2
			Total	**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table—2

Elective-II

Sr.No	Board Of Study	Subject Code	Subject
1	E&Tc	560233 (28)	Neural Network for VLSI
2	E&Tc	560212 (28)	VLSI System Testing
3	E&Tc	572231 (28)	ULSI Technology

Note (1) – 1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session.

Note (2) – Choice of elective course once made for an examination cannot be changed in future Examinations.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem
Subject: Mixed Signal and RF circuit Design
Total Theory Periods: 40
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

Branch: Electronics & Telecom
Specialization: VLSI & Embedded System Design
Code : 572211 (28)

Mixed Signal and RF circuit Design

Unit I: Basic Concepts in RF design : Nonlinearity and Time Variance, Intersymbol Interference, Random Processes & Noise , Sensitivity & Dynamic Range, Passive Impedance Transformation, Passive RLC Networks ,Characteristics of Passive IC Components.

Unit II: **Distributed Systems:-** Link between Lumped and Distributed Regimes, Driving Point Impedance, Finite Length Transmission Lines, Smith Chart, S parameter , Bandwidth Estimation Techniques:-Method of Open-Circuit & Short –Circuit Time Constants.

Unit III: Low Noise Amplifier :- General Consideration ,Input Matching ,CMOS LNAs ,CMOS Mixers,Noise in Mixers,Basic LC Oscillator Topologies, VCO,Phase Noise ,CMOS LC Oscillator ,Quadrature Signal Generation ,Single Sideband Generation.

Unit IV: Data Converters:- Specification of Converters,Flash Converter,Dual Slope A/D Converter, Pipelined & Sigma Delta Converter. D/A Converters, R-2R, Binary weighted ,Weighted Capacitor Converter System,Self Calibrating D/A Converter System.

Unit V: Frequency Synthesizers, Linearized PLL Models, Noise Properties of PLLs, Phase Detectors,Loop Filters ,Charge Pumps,RF Synthesizer Architecture, Frequency Divider.

Text Book:

1) *T. H. Lee, Design of CMOS Radio Frequency Integrated Circuits, Second Edition, CUP, 2004.*

2) R. J. van de Plassche, Integrated A-D and D-A Converters, Second Edition, Springer/Kluwer, 2003. (Cheap Edition)

3) B. Razavi, RF Microelectronics, IEEE Press.

Reference:

1. *B. Razavi, Monolithic Phase-locked Loops and Clock Recovery Circuits: Theory and Design, IEEE Press, 1996.*
2. *Baker, CMOS mixed signal circuit design.wiley eastern, ISBN 978-0-470-29026-2*

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem **Branch: Electronics & Telecom**
Subject: CMOS Digital Circuit Design **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 572212 (28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

UNIT – I Basic Electrical Properties of MOS circuits: MOS transistor operation in linear and saturated regions, MOS transistor threshold voltage, MOS switch and inverter, latch-up in MOS inverter; sheet resistance and area capacitances of layers, wiring capacitances;

UNIT – II CMOS inverter properties - robustness, dynamic performance, regenerative property, inverter delay times, switching power dissipation, MOSFET scaling - constant-voltage and constant-field scaling;

UNIT – III Dynamic CMOS design: steady-state behavior of dynamic gate circuits, noise considerations in dynamic design, charge sharing, cascading dynamic gates, domino logic, np-CMOS logic, problems in single-phase clocking, two-phase non-overlapping clocking scheme;

UNIT- IV Subsystem design: design of arithmetic building blocks like adders - static, dynamic, Manchester carry-chain, look-ahead, linear and square-root carry-select, carry bypass and pipelined adders and multipliers - serial-parallel, Braun, Baugh-Wooley and systolic array multipliers,

UNIT – V Barrel and logarithmic shifters, area-time tradeoff, power consumption issues; designing semiconductor memory and array structures: memory core and memory peripheral circuitry.

Texts:

1 *J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits- A Design Perspective, 2nd Ed, PHI, 2003.*
2 *D. A. Pucknell and K. Eshraghian, Basic VLSI Design, PHI, 1995.*
3 *E. D. Fabricius, Introduction to VLSI Design, McGraw Hill, 1991.*
4 *Stephen Brown, "Fundamentals of digital design with VHDL design"*

References:

1 *N. H. E. Waste and K. Eshraghian, Principles of CMOS VLSI Design - a System Perspective, 2nd Ed, Pearson Education Asia, 2002.*
2 *S. M. Kang and Y. Leblevici, CMOS Digital Integrated Circuits Analysis and Design, 3rd Ed, McGraw Hill, 2003.*
3 *J. P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons Pvt. Ltd, 2002.*
4 *W. Wolf, Modern VLSI Design - System on Chip design, 3rd Ed, Pearson Education, 2004.*
1. *R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, IEEE Press, 1997.978-0-470-29026-2*

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem
Subject: Digital Signal Processors
Total Theory Periods: 40
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

Branch: Electronics & Telecom
Specialization: VLSI & Embedded System Design
Code : 572213 (28)

Unit I: Computational characteristics of DSP algorithms: basic DSP operations; a generic instruction-set architecture for DSPs; architectural requirement of DSPs: techniques for enhancing computational throughput - parallelism and pipelining;

Unit II: Data-path of DSPs: multiple on-chip memories and buses, dedicated address generator units, specialized processing units (hardware multiplier, ALU, shifter). On-chip peripherals for communication and control; control-unit of DSPs: pipelined instruction interrupts;

Unit III: Architecture of Texas Instruments fixed-point and floating-point DSPs: architecture of TMS320C5x, C54x/C3x DSPs, Programmer's model, addressing modes, assembly language instructions; memory interfacing, parallel I/O interfacing; on chip peripheral: timer and serial port interface;

Unit IV: Description of TMS6xxx series; architecture of analog devices fixed-point and floating-point DSPs: brief description of ADSP 218x / 2106x DSPs; programmer's model; **Advanced DSPs:** TI's TMS 320C6x, ADI's Tiger-SHARC, Lucent Technologies' DSP 16000 VLIW processors;

Unit V: Multirate DSP: concept of multirate signal processing, Interpolation, Decimation, Filter for multirate, multirate DSP Application.

Texts

1. *P. Pirsch, Architectures for Digital Signal Processing, John Wiley, 1999.*
2. *R. J. Higgins, Digital Signal Processing in VLSI, Prentice-Hall, 1990.*
3. *Analog Devices ADSP 2100-family and 2106x-family Users Manuals.*
4. *K. Parhi, VLSI Digital Signal Processing Systems, John Wiley, 1999.*

References:

1. *K Parhi and T. Nishitani, Digital Signal Processing for Multimedia Systems, Marcel Dekker, 1999.*
2. *IEEE Signal Processing Magazine, Oct 88, Jan 89, July 97, Jan 98, March 98 and March 2000.*
3. *Texas Instruments TMSC5x, C54x and C6x Users Manuals*

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem **Branch: Electronics & Telecom**
Subject: Application Specific Integrated Circuits **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 572214 (28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

UNIT –I Introduction **to ASIC**, Modeling combinational and sequential circuits, Design entry by verilog / VHDL /FSM / SYSTEM C, Hardware modeling with Verilog / VHDL, different Verilog /VHDL constructs, and Logic Synthesis.

UNIT – II ASIC construction, Simulation ,Verification of complex logic design model, Verification issues like verification plan, verification methodology, timing verification, Hardware design verification, Software design verification ,verification strategy for ASIC bus functional models,

UNIT – III verification Automation, physical verification, Layout planning and verifications ,ASIC design flow and HDL based ASIC design flow, EDA tools for ASIC design, Mixed signal design , Introduction to VLSI physical design, floor planning , placement and routing parameter extraction ,

UNIT – IV Analysis: static timing analysis , current analysis , clock tree synthesis , power grid analysis , clock skew analysis and post layout synthesis , Data structure for graph models, , different tools for the PAR, Design rule and electric rule checking, LVS , Wire length / load estimator, stick diagrams by using
CMOS for various combination Ckt and Different timing parameters for ASICs.

UNIT V Test specification , need for testability, Boundary Scan Test , Faults , Fault simulation , Automatic Test pattern Generation , SCAN test , Built in Self test ,Gate level simulation and IC verification. Tools used for front to back end chip design.

Text books:

1. *Wayne Wolf, "Modern VLSI Design "by Pearson Education Asia*

2. Michael Smith,"Application Specific Integrated Circuits –"by Pearson Education Asia

References: .

1. *Geiger, Allen Strader,"VLSI Design Techniques for Analog and Digital circuits "McGraw HILL*
2. *Neil Waste," Principles of CMOS VLSI Design "by Pearson Education Asia*

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem **Branch: Electronics & Telecom**
Subject: Neural Networks for VLSI **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 560233 (28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

UNIT I
Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons

UNIT II
ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning.

UNIT III
Supervised Learning and Neurodynamics: Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

UNIT IV
Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ART networks, LVQ

UNIT V
Applications for VLSI Design: Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Text:
1. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999
2. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall
International,
New Jersey, 1999.
Reference:
1. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications andProgramming Techniques", Addison-Wesley, Reading, Mass, (1992).
2. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.
3. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem **Branch: Electronics & Telecom**
Subject: VLSI System Testing **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 560212 (28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

UNIT I

Special purpose Subsystems: Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc. **Design Economics:** Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Personpower, example

UNIT II

TESTING OF COMBINATIONAL CIRCUITS: Faults in digital circuits – Failures and faults –Modeling of faults – Temporary faults – Test generation for Combinational logic circuits – testable combinational logic circuit design – Scan based design and JTAG testing issues.

UNIT III

TESTING OF SEQUENTIAL CIRCUITS: Test generation for sequential circuits – Design of testable sequential CK5- Built in self test – Testable memory design.

UNIT IV

VERIFICATION AND TESTING: Verification – Timing verification – Testing concepts – Fault coverage – ATPG – Types of tests – Testing FPGAs – Design for testability.

UNIT V

VLSI System Testing & Verification: Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan. **VLSI Applications:** Case Study: RISC microcontroller, ATM Switch, etc.

Text:

1. Neil H.E. Weste, Davir Harris, “CMOS VLSI Design: A Circuits and system perspectives” Pearson Education 3rd Edition.
2. Wayne, Walf, “Modern VLSI design: System on Silicon” Pearson Education, Second Edition

References:

1. Pucknull, “Basic VLSI Design” PHI 3rd Edition

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem **Branch: Electronics & Telecom**
Subject: ULSI Technology **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 572231(28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

Unit I : Clean room Technology : Classification, Design concepts, Installation, Operation and Automation. **Wafer- Cleaning Technology:** Basic concepts, Wet-Cleaning and Dry-Cleaning Technology. Epitaxy: Fundamental Aspects, Conventional Si Epitaxy, Low temperature Epitaxy of Si, Selective Epitaxial Growth of Si.

Unit II : **conventional and Rapid thermal process**: Requirement of thermal process, Rapid thermal processing, **Dielectric and polysilicon film deposition:** Deposition process, APCVD & LPCVD silicon oxides, LPCVD silicon nitride, LPCVD Polysilicon film, Plasma assisted Deposition, Applications of deposited polysilicon, silicon oxide.

UNIT III : **Lithography and Etching:** Optical, Electron, X-ray , Ion lithography, Low pressure gas discharge, Etching mechanism, selectivity and profile control, Reactive plasma etching techniques and equipments, Plasma processing, Wet chemical etching. **Metallization:** Metal deposition technique, silicide process, CVD Tungsten plug and other plug process, Multilevel Metallization, Metallization Reliability,

UNIT IV: Process integration: Basic process module and devices consideration for ULSI, CMOS Technology, Bipolar technology, BiCMOS technology, MOS memory technology, Process integration consideration in ULSI Fabrication Technology. **Assembly & Packaging:** Package type, ULSI assembly technology, Package fabrication technology, package design consideration, Special package consideration.

UNIT V: Wafer Fab Manufacturing technology: Wafer Fab manufacturing consideration, manufacturing start-up technology, Volume ramp up Consideration, Continuous improvement. **Reliability:** Hot carrier injection, electromagnetism, stress migration, oxide breakdown, Effect of scaling on device reliability, Relation between DC and AC lifetime, Some recent ULSI Reliability concern, Mathematics of Failure distribution.

TEXT BOOK:

1. *C.Y. Chang and S. M. Sze "ULSI Technology" McGraw-Hill publications.*
2. *Chen, "VLSI Technology" Wiley, March 2003.*

REFERENCE BOOKS:

1. *B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.*
2. *Sze, "Modern Semiconductor Device Physics", John Wiley & Sons, 2000*

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem
Subject: CMOS Circuit Design Lab-I
Total Practical Periods: 40
Total Marks in End Semester Exam. : 75
Minimum number of class test to be conducted: 02

Branch: Electronics & Telecom
Specialization: VLSI & Embedded System Design
Code : 572221 (28)

Name of Experiments

1. Design and simulation of Common Source Amplifier.
2. Design and simulation of CMOS Inverter.
3. Design and simulation of Current Mirror.
4. Design and simulation of first stage of Opamp.
5. To draw layout of CMOS inverter
6. To draw layout of CMOS NAND gate.
7. To draw layout of CMOS NOR gate.
8. To draw layout using interdigitized and Common Centroid Method.
9. To draw layout of Resistance for a specific value.
10. To draw layout of Capacitor for a specific value..
11. To draw layout of a Differential amplifier.
12. To draw layout of a Current Mirror.

Note: Minimum 10 Experiments to be performed.

Extra experiments can be added if necessary.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIst Sem
Subject: DS Processor Lab-II
Total Practical Periods: 40
Total Marks in End Semester Exam. : 75
Minimum number of class test to be conducted: 02

Branch: Electronics & Telecom
Specialization: VLSI & Embedded System Design
Code : 572222 (28)

Lab Experiments

1. Design. of 16 bit adder & implementation using TMS 320C6X.
2. Design. of Algorithm to move a block from memory to register.
3. Design. & Implementation of a hardware multiplier using C Language programming.
4. Study of pipe line instruction use in processing of data with the help of interrupts.
5. Design. & Implementation of butter worth digital IIR filter by bl linear transformation method using TMS 320 C6 X.
6. Design. Of chebeshev Digital IIR filter using bi linear transformation with TMS 320C6X.
7. Design. Of FIR Digital filter by hanning or hamming window with the help of TMS 320C5X / C6X.
8. Write on Algorithm to implement & process a filter speech signal at required frequency using any Digital Signal Processor.
9. Write on assembly language code to control stepper motor by standard Digital Signal Processor.
10. Write an algorithm to implement a simple diameter & Interpolator using standard Digital Signal Processor.

Note: Minimum 10 Experiments to be performed.

Extra experiments can be added if necessary.