Chhattisgarh Swami Vivekanand Technical University, Bhilai

SCHEME OF MASTER OF TECHNOLOGY

Electronics & Telecommunication Engineering (VLSI & Embedded System Design)

M. Tech. [Third Semester]

Sr. No.	Board Of Studies	Code	Subject	Weekly Teaching hours			Scheme of Examination			Grand Total	Credits
				L	T	P	ESE	CT	TA		
1	E&Tc	572311(28)	ARM Processor and controller	3	1	--	100	20	20	140	4
2	E&Tc	Elective III		3	1	--	100	20	20	140	4
3	E&Tc	572321(28)	Preliminary Work on Dissertation	--	--	28	100	--	100	200	14
4	E&Tc	572322(280	Seminar on Industrial Training & Dissertation	--	--	3	--	--	20	20	2
Total				**6**	**2**	**31**	**300**	**40**	**160**	**500**	**24**

Table—3
Elective-III

Sr.No	Board Of Study	Subject Code	Subject
1	**Electronics & Telecom**	560331 (28)	Algorithm for VLSI Design Automation
2	**Electronics & Telecom**	572331(28)	Electromagnetic Interference and Compatibility in system Design
3	**Electronics & Telecom**	572332(28)	VLSI signal processing.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIIrd Sem
Subject: ARM Processor and controller
Total Theory Periods: 40
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

Branch: Electronics & Telecom
Specialization: VLSI & Embedded System Design
Code : 572311(28)

ARM Processor and Controller

UNIT I
Introduction to 16 / 32-bit Micro controllers: ARM 7/ARM 9 architecture, ARM Microcontrollers and Processor Cores, ARM Architecture and Organization, ARM/THUMB Programming Model, ARM/THUMB Instruction Set , ARM Exception Handling ,More ARM Instructions, ARM/THUMB Assembly Programming

UNIT II
Data handling, interfacing with Memory, Interrupts, Timers, ARM Bus. I/O Devices, Controllers, Simple & Autonomous I/O Controllers,

UNIT III
Parallel, Multiplexed, Tristate, and Open-Drain Buses, Bus Protocols, Serial Transmission Techniques & Standards, Wireless protocols CAN & advanced Buses.

UNIT IV
Design Methodology, Design Flow, Architecture Exploration, Functional Design, Functional Verification, Synthesis, Physical Design,

UNIT V
Design Optimization, Area Optimization, Timing Optimization, Power Optimization, Design for Test , Fault Models and Fault Simulation, Scan Design and Boundary Scan, Built-In Self Test (BIST), Nontechnical Issues.

BOOKS

1. *Data books of ARM7/ARM9 J. Staunstrup and W. Wolf, editors, Hardware/Software Co-Design: Principles and Practice, Kluwer Academic Publishers, 1997.*

Reference:

1. ARM System-on-Chip Architecture, by Steve Furber ,Pearson Education **Edition:** 2nd
2. *Arm System Developer'S Guide: Designing And Optimizing System Software (Paperback)* by Sloss Andrew N. Et.Al, **Publisher:** Morgan Kaufmann Publishers **Edition:** 1st

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIIrd Sem **Branch: Electronics & Telecom**
Subject: Algorithm for VLSI Design Automation **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 560331(28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

Algorithm for VLSI Design Automation

UNITI
Logic synthesis & verification: Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT II
VLSI automation Algorithms: Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms. Placement, floor planning & pin assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor plannning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT III
Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

UNIT IV
Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT V
Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization. Compaction: problem formulation, one-dimensional compaction, two dimension-based compaction, hierarchical compaction

Text:
1. Naveed Shervani, “Algorithms for VLSI physical design Automation”, Kluwer Academic Publisher, Second edition.
2.Trimburger,” Introduction to CAD for VLSI”, Kluwer Academic publisher, 2002
References:
1. Christophn Meinel & Thorsten Theobold, “Algorithm and Data Structures for VLSI Design”, KAP,2002.
2. Rolf Drechsheler : “Evolutionary Algorithm for VLSI”, Second edition

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIIrd Sem **Branch: Electronics & Telecom**
Subject: Electromagnetic Interference and Compatibility in system Design **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 572331(28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

UNIT 1

EMI Environment
Sources of EMI conducted and radiated EMI, transient EMI, EMI-EMC definitions and units of parameters.

UNIT 2

EMI Coupling Principles
Conducted, radiated and transient coupling, common independence ground coupling, radiated common mode and ground loop coupling, radiated differential mode coupling, near field cable to cable coupling, power mains and power supply coupling.

UNIT 3
EMI Specification/Standards & Measurements
Unit of specifications, civilian standards military standards. EMI test instruments/systems, EMI test, EMI Shielded chamber, open area test site, TEM Cell antennas, conductors injectors/couplers, military test method and procedures, calibration procedures.

UNIT 4

EMI Control Techniques
Shielding, filtering, grounding, bonding, isolation transformer, transient suppressors, cable routing, signal control, component selection and mounting.

UNIT 5

EMC Design of PCBs
PCB traces cross talk, impedance control, power distribution decoupling, zoning, motherboard designs and propagation delay performance models.

Books:

1. *Bernhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, 3rd Ed., 1986.*

Reference:

1. *Henry W.Ott, "Noise Reduction Techniques in Electronic Systems", John wiley and Sons. 1988.*

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: M. Tech. IIIrd Sem **Branch: Electronics & Telecom**
Subject: VLSI Signal Processing **Specialization: VLSI & Embedded System Design**
Total Theory Periods: 40 **Code : 572332(28)**
Total Marks in End Semester Exam. : 100
Minimum number of class test to be conducted: 02

VLSI Signal Processing (Elective III)

UNIT 1
Introduction to DSP systems – Iteration Bound – Pipelined and parallel processing.

UNIT 2
Retiming – unfolding – algorithmic strength reduction in filters and transforms.

UNIT 3
Systolic architecture design – fast convolution – pipelined and parallel recursive and adaptive filters.

UNIT 4
Scaling and round off noise – digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic.

UNIT 5
Numerical strength reduction – synchronous, wave and asynchronous pipe lines – low power design – programmable digit signal processors.

Book:

1. *Keshab K. Parthi, "VLSI Digital signal processing systems, design and implementation", Wiley, Inter Science, 1999.*
2. *Mohammad Isamail and Terri Fiez, "Analog VLSI signal and information processing", Mc Graw – Hill*
3. *S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.*

Reference:

4. *Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994*