Chhattisgarh Swami Vivekanand Technical University, Bhilai

Scheme of Teaching and Examination

B.E. VI Semester

Electronics & Telecommunication Engineering

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Board of Study</th>
<th>Code No.</th>
<th>Subjects</th>
<th>Period Per Week</th>
<th>Scheme of Exam</th>
<th>Total Marks</th>
<th>Credit</th>
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<tr>
<td></td>
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<td>328651(28)</td>
<td>Digital Signal Processing</td>
<td>L  3 T  1 P -</td>
<td>Theory/ Practical</td>
<td>80 20 20 120 4</td>
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<td>328652(28)</td>
<td>Electronic Circuit Design</td>
<td>L  3 T  1 P -</td>
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<td>L  3 T  1 P -</td>
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<td>328655(28)</td>
<td>Information Theory &amp; Coding</td>
<td>L  3 T  1 P -</td>
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<td>Digital Signal Processing Lab</td>
<td>L  - T  - P 2</td>
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<td>Theory/ Practical</td>
<td>40 - 20 60 2</td>
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<td></td>
<td>Management</td>
<td>300665(76)</td>
<td>Managerial Skills</td>
<td>L  - T  - P 2</td>
<td>Theory/ Practical</td>
<td>40 - 20 60 1</td>
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<td>L  - T  - P 1</td>
<td>Theory/ Practical</td>
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</tbody>
</table>

TOTAL: 18 5 17 640 120 240 1000 31

L: Lecture  T: Tutorial  P: Practical  ESE: End Semester Examination  CT: Class Test  TA: Teachers’ Assessment

Note: Industrial Training of eight weeks is mandatory for B.E. students. It is to be completed in two equal parts. The first part must have been completed in summer after IV semester. The second part to be completed during summer after VI semester after which students have to submit a training report which will be evaluated by college teachers during B.E. VII semester.

Table 1

Professional Elective – I

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Board of Study</th>
<th>Code No.</th>
<th>Subject</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>Electronics &amp; Telecom.</td>
<td>328671(28)</td>
<td>Internet &amp; Web Technology</td>
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<tr>
<td>2</td>
<td>Electronics &amp; Telecom.</td>
<td>328672(28)</td>
<td>Operating System</td>
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<tr>
<td>3</td>
<td>Electronics &amp; Telecom.</td>
<td>328673(28)</td>
<td>Biomedical Electronics</td>
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<td>5</td>
<td>Electronics &amp; Telecom.</td>
<td>328675(28)</td>
<td>Computer Organization &amp; Architecture</td>
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<tr>
<td>6</td>
<td>Electronics &amp; Telecom.</td>
<td>328676(28)</td>
<td>Advanced Semiconductor Devices</td>
</tr>
</tbody>
</table>

Note:
1. 1/4th of total strength of students to minimum of twenty students is required to offer an elective in the college in a particular academic session
2. Choice of elective course once made for an examination cannot be changed in future examinations.

Name of the Programme: Bachelor of Engineering  Duration of the Programme: Four Years
## Course objective:
- To study the basic mathematical techniques needed for analysis of discrete time signals and systems.
- To study the various digital filter design techniques.
- To study the multirate digital signal processing techniques.

## Course Outcomes:
At the end of this course students will demonstrate the ability to:
1. Synthesize discrete time signals from analog signals.
2. Use time domain and frequency domain analysis tools.
3. Apply forward and reverse transformations.
4. Visualize various applications of DSP and explore further possibilities.
5. Design IIR and FIR filters.

### UNIT I Analysis of Discrete Time Signals and Systems:

### UNIT II Implementation of Discrete-time Systems:

### UNIT III FIR Filter Design:
Symmetric and Anti-symmetric FIR filters, FIR Filter design by window method (Rectangular, Bartlett, Hamming, Hanning, Blackman and Kaiser window), Frequency Sampling method, Optimum approximation of FIR filters, Design of FIR differentiators, Design of Hilbert transformers.

### UNIT IV IIR Filter Design:

### UNIT V Multirate Digital Signal Processing:
Introduction, Decimation, Interpolation, Sampling rate conversion by rational factor, Filter design and implementation for sampling rate conversion: Direct form FIR digital filter structure, Polyphase filter structure, Time varying digital filter structure, Sampling rate conversion by an arbitrary factor.

### Name of Text Books:

### Name of Reference Books:
Name of the Programme: Bachelor of Engineering

Duration of the Programme: Four Years

Course objectives:
1. To become familiar with fundamental electronic circuits.
2. To learn to use common wave shaping Circuits.
3. To become familiar with Timer circuits designing for applications.
4. To be able to design active filter electronic circuits to perform realistic tasks.

Course Outcome:
1. To understand electronics waveshaping circuits.
2. The student will be able to understand timer IC and Its Applications and Design concepts
3. Student will be able to understand Designing concepts of Active filters.


UNIT II Multivibrators: Transistor as Switch, Types of Multivibrator (bistable, astable & monostable), Fixed and self biased binary, use of Commutating Capacitor, improving resolution, Schmitt trigger Emitter Coupled ,Monostable and Astable Multivibrator : Collector – Coupled and Emitter – Coupled Multivibrator.


Name of Text Books:
1. Pulse, Digital and Switching Waveforms by Millman & Taub, TMH Publishing Co.(Unit-1,2)
3. Analog Filter Design; Van –Valkenburg ; Holt –Standers International Edn. (Unit-4,5)

Name of Reference Books:
1. Operational Amplifiers and Linear Integrated Circuits, Coughlin and Driscoll, 6th Ed., PHI
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Course: Microcontroller & Embedded System

Course Code: 328653(28)

Duration: Three Hours
Maximum Marks in ESE: 80 Minimum Marks in ESE: 28

Course objectives:
- To make students familiar with the basic blocks of microcontroller device and Embedded system in general.
- To provide comprehensive knowledge of the architecture, features and interfacing with 8051 microcontroller.
- To use assembly and high level languages to interface the microcontrollers to various applications.

Course Outcome:
1. To understand Microcontroller 8051 its architecture and its instruction set.
2. Gain knowledge about Counter/timer and interrupts in 8051 Microcontroller and Programming concepts.
3. Students will be able to do serial communication programming and gain knowledge of serial communication.
4. Students will be able to understand interfacing Microcontroller 8051 with devices.

UNIT I  Introduction to Microcontroller: A brief History of Microcontrollers, Harvard Vs Von-Neumann Architecture; RISC Vs CISC, Classification of MCS-51family based on their features ( 8051,8052, 8031, 8751, AT89C51 ), Pin configuration of 8051.

8051 Processor Architecture and Instruction Set: Registers of 8051, Inbuilt RAM, Register banks, stack, on-chip and external program code memory ROM, power reset and clocking circuits, I/O port structure, Addressing modes, Instruction set and programming.

UNIT II  Counter/Timer and Interrupts of 8051: Introduction, Registers of timer/counter, Different modes of timer/counter, Timer/counter programming, Interrupt Vs Polling, Types of interrupts and vector addresses, register used for interrupts initialization, programming of external interrupts, Timer interrupts.


UNIT IV  Interfacing with 8051: Interfacing and programming of: ADC (0804,0808/0809,0848) & DAC (0808), stepper motor, 4x4 keyboard matrix, Relays, LED and Seven segment display, LCD, Interfacing (only) of different types of Memory, Address decoding techniques


Names of Text Books:
1. The 8051 Microcontroller and Embedded Systems using Assembly and C, Mazidi, Mazidi & McKinlay, 2nd Ed.,PHI.(Unit-I,II,III)
2. Embedded system, Frank Vahid.(Unit-IV)

Names of Reference Books:
2. 8 bit Microcontrollers & Embedded Systems Manual.
3. Programming and Customizing the 8051 Microcontroller, Predko; TMH
Chhattisgarh Swami Vivekanand Technical University, Bilai

Name of the Programme: Bachelor of Engineering

Duration of the Programme: Four Years

Branch: Electronics & Telecommunication Engineering  Semester: VI
Subject: VLSI Design  Code: 328654(28)
Total Theory Periods: 40  Total Tutorial Periods: 12
No. of class Tests to be conducted: 2 (Minimum)  No. of assignments to be submitted: 2 (Minimum)
ESE Duration: Three Hours  Maximum Marks in ESE: 80  Minimum Marks in ESE: 28

Course Objectives:
1. To understand the IC design aspects, basic fabrication steps.
2. To study the design rules & representation of circuits at lower level of abstraction.
3. To understand the layout design of few combinational and sequential circuits.
4. To study one of the HDL (hardware description language) for front end design.
5. To study internal structure of programmable logic devices.

Course Outcomes:
1. Students are expected to understand CMOS fabrication details.
2. Students are expected to understand schematic, layout of combinational circuits.
3. Students are expected to understand schematic, layout of sequential circuits.
4. Students are expected to understand VHDL programming concepts.

UNIT I  An Overview & Analysis of CMOS Integrated Circuits: Complexity and Design: Design Flow, VLSI Chip Types, Moore’s Law; MOSFETs as Switch: FET Threshold Voltages, Pass Characteristics; Basic Logic Gates in CMOS: NOT Gate, NOR Gate, NAND Gate; Complex Logic Gates in CMOS: Structured Logic Design, XOR and XNOR Gates; Transmission Gate Circuits: Multiplexers, OR Gate, XOR/XNOR Gate, DC characteristics of the CMOS inverter, Switching Characteristics: Fall Time, Rise Time, Propagation Delay; Power Dissipation.

UNIT II Fabrication & Physical Design of CMOS Integrated Circuits: CMOS Layers; Designing FET Arrays; Basic Gate Designs; Complex Logic Gates; Euler Graph; Overview of Silicon Processing; Material Growth and Deposition; Lithography; CMOS Process Flow; CMOS Design Rules; Layout of Basic Structures: nWell, Active Areas, Doped Silicon Regions, MOSFETs, Active Contacts, Metal, Vias; Physical Design(Stick diagram &Layout Design) of Logic Gates: NOT, NAND & NOR.

UNIT III CMOS Subsystem Design: Schematic and Layout of CMOS Combinational Circuits: Full adder circuit, Multiplexer, Parity Generator, Schematic and Layout of CMOS Sequential Circuits: SR Flip-Flop, JK Flip-Flop, & D Flip-Flop, 4x4 NOR based ROM Array, 4x4 NAND based ROM Array; Schematic of SRAM and operation of DRAM: 3-T DRAM 6-T DRAM;


Textbooks:
1. Introduction to VLSI Circuits and Systems: John P. Uyemura, John Wiley & Sons (Unit-I & II).
2. CMOS Digital Integrated Circuits: Analysis & Design; Sung-Mo Kang & Yusuf Leblebici, TMH, (Unit-III)
4. VHDL Primer by J. Bhaskar, PHI(Unit-IV & V)

Reference Books:
3. CMOS circuit design, layout and simulation by Jacob Baker, PHI
**Chhattisgarh Swami Vivekanand Technical University, Bhilai**

| Name of the Programmes: | Bachelor of Engineering
<table>
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<tbody>
<tr>
<td><strong>Branch:</strong></td>
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<tr>
<td><strong>Subject:</strong></td>
<td><strong>Information Theory &amp; Coding</strong></td>
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<tr>
<td><strong>Semester:</strong></td>
<td>VI</td>
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<td><strong>Code:</strong></td>
<td>328655(28)</td>
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<td><strong>Total Theory Periods:</strong></td>
<td>40</td>
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<tr>
<td><strong>Total Tutorial Periods:</strong></td>
<td>12</td>
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<tr>
<td><strong>No. of class Tests to be conducted:</strong></td>
<td>4 (Minimum)</td>
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<td><strong>No. of assignments to be submitted:</strong></td>
<td>2 (Minimum)</td>
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<td><strong>ESE Duration:</strong></td>
<td>Three Hours</td>
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<td><strong>Maximum Marks in ESE:</strong></td>
<td>80</td>
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<tr>
<td><strong>Minimum Marks in ESE:</strong></td>
<td>28</td>
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</table>

**Course Objectives:**
- To learn about various source coding and channel coding techniques.
- To study various error control coding techniques.
- To Gain knowledge about BCH code and implementation of RS encoder and decoder.
- To learn convolutional coding, viterbi decoding and turbo codes.
- To gain knowledge about Trellis Coded Modulation

**Course Outcomes:**
1. Students will be able to understand the concept of various Source Coding Techniques and Channel Coding Techniques.
2. Students will be able to analysis various error control coding techniques.
3. Students will be able to understand BCH Code and RS Code.
4. Students will get the knowledge of convolutional Code.

**UNIT I**  
**Channel Capacity Coding** : Channel Models, Channel Capacity, Channel Coding, Information Capacity Theorem, The Shannon Limit.

**UNIT II**  
**Error Control Coding (Channel Coding) Linear Block Codes for Error Correction & Cyclic Codes** : Introduction to Error Correcting Codes, Basic Definitions, Matrix Description of Linear Block Codes, Equivalent Codes, Parity Check Matrix, Decoding of a Linear Block Code, Syndrome Decoding, Hamming Codes.  
**Cyclic Codes** : Polynomials, The Division algorithm for Polynomials, A Method for Generating Cyclic codes, Matrix Description of cyclic codes, Burst Error Correction.

**UNIT III**  
**Bose-Chaudhuri Hocquenghem (BCH) Codes** : Introduction to BCH Codes, Primitive Elements, Minimal Polynomials, Generator Polynomials in Terms of Minimal Polynomials, some Examples of BCH Codes, Decoding of BCH Codes, Introduction to Reed-Solomon Codes,  

**UNIT IV**  
**Convolutional Codes** : Introduction to Convolutional Codes, Tree codes and Trellis Codes, Polynomial Description of Convolutional Codes (analytical Representation), distance Notions for Convolutional Codes, The Generating Function, Matrix Description of Convolutional Codes, Viterbi Decoding, Distance Bounds for Convolutional Codes.

**UNIT V**  

**Name of Text Books:**
1. Information Theory coding & Cryptography by Rajan Bose,(Unit- I,II,III,IV,V) Tata McGraw-Hill,
3. Digital communication - Sklar, Pearson Publication
4. Digital communication - Prokais, Tata McGrawHill

**Name of the Programme: Bachelor of Engineering  Duration of the Programme: Four Years**
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch: Electronics & Telecommunication Engineering  
Subject: Digital Signal Processing Laboratory

Total Lab Periods: 36  
Maximum Marks: 40

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To generate the basic Analog and Discrete Signals.
2. Implementation of Linear convolution, Circular convolution, Linear convolution using circular convolution.
3. DFT Implementation for a given signal.
4. To plot Fourier Transform amplitude spectrum and phase spectrum for a given function.
5. To plot frequency response in Z-domain for the given transfer function.
6. To plot frequency response in S-domain for a given transfer function.
7. To sample a sinusoidal signal at Nyquist rate, above the Nyquist Rate and below the Nyquist Rate.
8. Design & implementation of IIR filters [LPF, HPF, BPF, BSF].
9. Design & implementation of FIR filters [LPF, HPF, BPF, BSF].
10. Design various filters using Simulink.
11. To design a Graphical User Interface to display various basic signals [sine wave, sinc wave, etc].
12. To perform Interpolation and decimation [Multirate DSP].
13. To design a digital notch filter and embed it on a digital signal processor block.

(Institutes may append more programmes / Experiments based on the infrastructure available)

List of Equipments/Machine Required:
C++ Compiler, Simulation Software, DSP Processor kit, Digital Storage CRO, Spectrum Analyzer.

Recommended Books:
1. Digital Signal Processing, Vallavaraj, Salivahanan, Gnanapriya, TMH
2. Stein, J. Digital Signal Processing - a computer science perspective. Wiley

Name of the Programme: Bachelor of Engineering  
Duration of the Programme: Four Years
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Name of program: Bachelor of Engineering in Electronics & Telecommunication
Subject: Electronic Circuit Design Laboratory

Duration of the Programme: Four Years

Branch: Electronics
Semester: VI
Code: 328662(28)

Total Lab Periods: 36
Batch Size: 30
Maximum Marks: 40
Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To design clipper circuits to clip positive, negative and also clipping at two independent levels.
2. To design Clamper circuits.
3. To design a Bistable multivibrator circuit and to draw its output waveform.
4. To design a Monostable multivibrator circuit and to draw its output waveform.
5. To design an Astable multivibrator circuit and to draw its output waveform.
6. To design an astable multivibrator using 555 timer
7. To design a monostable multivibrator using 555 timer.
8. To design a LPF using R & C and to study its characteristics
9. To design a HPF using R & C and to study its characteristics
10. To design a BPF using R & C and to study its characteristics
11. To design Chebyshev filter using OPAMP and to plot its frequency response.
12. To design All Pass filter using OPAMP and to plot its frequency response.
13. To design Band-pass filter using OPAMP and to plot its frequency response.
14. To design HPF using OPAMP.
15. To design LPF using OPAMP.
16. To design HPF (Multistage) using OPAMP.

List of Equipments/Machine Required:
Discrete Components, Function Generator, Power Supply, CRO, AVO Meter, Multimeter, Voltmeter

Recommended Books:
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Name of program: Bachelor of Engineering  
Branch: Electronics & Telecommunication  
Subject: Microcontroller & Embedded System Laboratory  
Semester: VI  
Code: 328663(28)

List of Experiments: (At least Ten experiments are to be performed by each student)

1. Write a microcontroller 8051 program to transfer the bytes into RAM locations starting at 50H, assuming that ROM space starting at 240H contains CHHATTISGARH by using – a) Counter, b) nullchar. for end of string.

2. Write a microcontroller 8051 program to get hex data on the range of 00-FFh from port 0 and convert ito decimal. Save the digits in R7, R6 and R5, where the least significant digit is in R7.

3. Write a microcontroller 8051 program to add two 16 Bit unsigned numbers. Operands are two RAM variables. Results to be in R1-R0 pair.

4. Write a microcontroller 8051 program to subtract an unsigned 16 Bit number from another. Operands are two RAM variables. Results to be in R1-R0 pair.

5. Write a microcontroller 8051 program to add two unsigned 32-bit numbers. Operands are two RAM variables. Results to be in R1-R0 pair.

6. Write a microcontroller 8051 program to add two 16 Bit signed numbers.

7. Write a microcontroller 8051 program to convert a binary number to equivalent BCD

8. Write a microcontroller 8051 program to convert a packed BCD number to two ASCII numbers and place them in R5 and R6.

9. Write a microcontroller 8051 program to calculate the square root of an 8-bit number using iterative method.

10. Write a microcontroller 8051 program that generates 2kHz square wave on pin P1.0, 2.5 kHz on pin P1.2 and 25 Hz on pin P1.3.

11. Write a microcontroller 8051 program for counter 1 in mode 2 to count the pulses and display the state at the TL1 count on P2. Assume that the clock pulses are fed to pin T1.

12. Write a microcontroller 8051 program to transfer letter “N” serially at 9600 baud, continuously. Assume crystal frequency to be 11.0592 MHz.

13. Write a microcontroller 8051 program to transfer word “CSVTU” serially at 4800 baud and one stop bit, continuously. Assume crystal frequency to be 11.0592 MHz.

14. Write a microcontroller 8051 program to receive bytes of data serially, and put them in P1. Set the baud rate at 2400 baud, 8-bit data, and 1 stop bit. Assume crystal frequency to be 11.0592 MHz.

List of Equipments/Machine Required:

Microcontroller kit, Interfacing kit, Keyboard, Monitor, SMPS for Microcontroller
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Name of the Programme: Bachelor of Engineering

Electronics

Branch: &Telecommunication

Subject: VLSI Design Laboratory

Duration of the Programme: Four Years

Name of the Program Bachelor of Engineering

Semester: VI

Code: 328664(28)

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Total Lab Periods: 36

Maximum Marks: 40

Minimum Marks: 20

Batch Size: 30

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To Study Architecture of CPLD
2. To Study Architecture of FPGA
3. To Design Half Adder in Data Flow Style of Modeling and Implement it in the CPLD.
4. To Design Full Adder in Structural Style of Modeling and Implement it in the FPGA.
5. To Design 4:1 Multiplexer in Behavioral Modeling and Implementation in CPLD.
6. To Design 16:1 Multiplexer using Generate statement and Implementation in FPGA.
7. To Design 8bit adder using Generic statement and Implementation in CPLD.
8. To Design D Flip-Flop in Behavioral Modeling.
11. To Prepare and Verify the Layout for NOT Gate.
12. To Prepare and Verify the Layout for NAND Gate.
13. To Prepare and Verify the Layout for NOR Gate.
14. To Prepare the Layout for D-FF.
15. To Prepare the Layout for the logic equation (a * (b+c))’

EDA Tools to be used:

Front End: Modelsim, FPGA Advantage, Xilinx, EdWinXP, ActiveHDL.
Back End: Cadence, Zeni-EDA, Calibre, Tanner, Synopsis, H-Spice

CPLD: XC9572, XC95108 FPGA: XC3S400
**Chhattisgarh Swami Vivekanand Technical University, Bhilai**

Name of Program: Bachelor of Engineering  
Branch: Common to All Branches  
Subject: Managerial Skills  
No. of Lectures: 2/Week  
Total Marks in ESE: NIL  
Minimum number of Class Tests to be conducted: Two

<table>
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<tr>
<th>Name of Program: Bachelor of Engineering</th>
<th>Branch: Common to All Branches</th>
<th>Subject: Managerial Skills</th>
<th>No. of Lectures: 2/Week</th>
<th>Total Marks in ESE: NIL</th>
<th>Minimum number of Class Tests to be conducted: Two</th>
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<tr>
<td>Semester: VI</td>
<td>Code: 300665 (76)</td>
<td>Tutorial Period: NIL</td>
<td>Marks in TA: 40</td>
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**Objective:**
The course is introduced to develop managerial skills tremendously and enrich the abilities to enable one to meet the challenges associated with different job levels. Managerial skills are essential for overall professional development of an individual apart from gaining technical knowledge in the subject.

**Course Objectives**
Upon completion of this course, the student shall be able
- To define and explain the concept of managerial, written and oral communication skill;
- To understand the leadership skill;
- To develop self-appraisal and understand distinction between leader and manager;
- To develop positive attitude and thinking; and
- To understand managerial functions and develop creativity.

**UNIT I Managerial Communication Skills:** Importance of Business Writing: writing business letters, memorandum, minutes, and reports- informal and formal, legal aspects of business communication, oral communication- presentation, conversation skills, negotiations, and listening skills, how to structure speech and presentation, body language.

**UNIT II Managerial skills - Leadership:** Characteristics of leader, how to develop leadership; ethics and values of leadership, leaders who make difference, conduct of meetings, small group communications and Brainstorming, Decision making, How to make right decision, Conflicts and cooperation, Dissatisfaction: Making them productive.

**UNIT III Proactive Manager:** How to become the real you: The journey of self-discovery, the path of self-discovery, Assertiveness: A skill to develop, Hero or developer, Difference between manager and leader, Managerial skill check list, team development, How to teach and train, time management, Stress management, Self-assessment.

**UNIT IV Attitudinal Change:** Concept of attitude through example, benefits of right attitude, how to develop habit of positive thinking, what is fear? How to win it? How to win over failure? How to overcome criticism? How to become real you? How to Motivate? How to build self confidence?

**UNIT V Creativity:** Creativity as a managerial skill. Trying to get a grip on creativity. Overview of Management Concepts: Function of Management: Planning, organizing, staffing, controlling.

**Course Outcome**
- The students will be able to develop formal and informal, negotiation, written and oral communication skill;
- The students will be able to develop manage groups, resolve conflicts and leadership skill and decision making qualities;
- The students will be able to develop self-appraisal, teaching, training and managing stress and time;
- The students will be able develop positive thinking, motivating team members and winning race; and
- The students will be able to develop creativity and fundamental management functions.

**Text Books:**

**Reference Books:**
1. How to develop a pleasing personality by Atul John Rego, Better yourself books, Mumbai,2006
2. The powerful Personality by Dr. Ujjawal Patni & Dr. Prapat Deshmukh, Fusion Books, 2006
3. How to Success by Brian Adams, Better Yourself books, Mumbai, 1969

Name of the Programme: Bachelor of Engineering  
Duration of the Programme: Four Years
Course objective:
1. To provide the fundamental concepts of Internet and to make students recognize the difference between various Internet protocols.
2. To introduce the concept of e-mail, list server & file transfer protocols.
3. To introduce the concept of HTML, Javascript & XML.
4. To introduce the concept of Internet security, Firewalls, E-commerce & EDI.

Course Outcome:
1. Students will be familiar with various Internet protocols and the concepts of Internet.
2. Students will able to differentiate between various e-mail protocols and their working.
3. Students will be familiar with the concept of remote login with the understandability of hosting and maintaining of website.
4. Students will also get knowledge about Internet security and Firewalls.


UNIT III  XML: What is XML – Basic Standards, Schema Standards, Linking & Presentation Standards, Standards that build on XML, Generating XML data, Writing a simple XML File, Creating a Document type definition, Documents & Data ,Defining Attributes & Entities in the DTD ,Defining Parameter Entities & conditional Sections, Resolving a naming conflict, Using Namespaces, Designing an XML data structure,Normalizing Data, Normalizing DTDS.


Text Books:
1. Internet & Intranet Engineering.- Daniel Minoli, TMH.
2. Alexis Leon and Mathews Leon – Internet for Every One, Tech World.

Reference Books:
Chhattisgarh Swami Vivekanand Technical University, Bhilai

**Branch:** Electronics & Telecommunication Engineering
**Subject:** Operating System (Professional Elective – I)
**Semester:** VI
**Code:** 328672(28)

<table>
<thead>
<tr>
<th>Total Theory Periods:</th>
<th>40</th>
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<tbody>
<tr>
<td>No. of class Tests to be conducted:</td>
<td>2 (Minimum)</td>
</tr>
<tr>
<td>ESE Duration:</td>
<td>Three Hours</td>
</tr>
<tr>
<td>Maximum Marks in ESE:</td>
<td>80</td>
</tr>
<tr>
<td>Minimum Marks in ESE:</td>
<td>28</td>
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</table>

**Course objective:**
1. To provide an understanding of the functions of operating systems.
2. To provide an insight into internals and functional modules of operating systems.
3. To study the concepts underlining the design and implementation of memory management of operating systems.
4. To make student able to understand deadlocks and to recover them.
5. To make student understand the core structure, functions and design principles of distributed operating system will be introduced with this subject.

**Course Outcome:**
1. The student will be able to learn the various functionalities of OS.
2. The student will be able to use the various algorithms and techniques to perform the various jobs performed by operating systems.
3. The student will be able to get the overview of how operating system is designed.
4. The student will be able to demonstrate how various resources are managed by operating system.

**UNIT I**  
**Introduction to operating system:** Functions provided by operating system, Introduction to multi programming, Time sharing and real time systems, Introduction to file systems, Access and allocation methods of file systems, Directory structure of a file system on a disk and tape, File protection.

**UNIT II**  
**Introduction to scheduling:** Process concept, states of process, Process control block, CPU scheduling, various types of CPU scheduling algorithms and their evaluation. Meaning of disk and drum scheduling. Various types of disk and drum scheduling algorithms like FCFS, SCAN etc., CPU protection.

**UNIT III**  
**Introduction to memory management:** Various types of memory management schemes like paging, Segmentation etc. Concept of virtual memory, demand paging, Various page replacement algorithms, thrashing and methods to tackle it, Memory protection.

**UNIT IV**  
**Concurrency and Deadlock:** Meaning of deadlocks, Resource allocation graphs, Deadlock Characterization, Various methods to avoid deadlocks like deadlock avoidance, Deadlock detection, Deadlock prevention, Banker’s algorithm for deadlock avoidance. Introduction to concurrent processing, Precedence graphs, Critical section problem, Semaphore concept, Study of classical process co-ordination problem.

**UNIT V**  

**Text Books:**
1. Operating System Concepts, James L. Peterson and Abraham Silberschatz (Addison-Wesley)
2. Modern Operating System, Andrew S. Tanenbaum, PHI

**Reference Books:**
1. Operating System Concepts & Design, Milan Milenkovic (MGH)
2. An Introduction to Operating Systems, Harvey M. Dietel(Addison Wesley)
Course objective:
1. To provide an understanding the function of Man Instrument System.
2. To provide an understanding of the heart and cardiovascular system and measurement of parameters involved.
3. To know the methods of measurements of various Biological parameters.
4. To make student understand the devices used and medical equipment used in patient-care and monitoring.
5. To know about Biotelemetry and its application in patient care.

Course Outcome:
1. Student will be able to understand problem found un measuring a living system.
2. Student will get an idea of Bio-electric potentials in cardio vascular system
3. Student will be able to understand measurement of Biological Parameters..
4. Student will be able to understand. Application of Telemetry and various equipment used in patient care.


UNIT IV Patient Care and Monitoring: The Elements of Intensive Care Monitoring, Pacemakers, Defibrillators, Heart Lung Machine, CT scan system, MRI scan system, Electrical Safety of Medical Equipment.


Name of Text Books:

Name of Reference Books:
1. Electronics in Medicine and Biomedical Instrumentation – Nandini K. Jog, PHI
2. Biomedical Instrumentation – Dr. A. Arumugam, Anuradha Agencies, Chennai.
4. Introduction to Biomedical Engineering, Domach, Pearson Education
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch: Electronics & Telecommunication Engineering
Subject: Electronic Engineering Materials & Components
(Professional Elective – I)
Semester: VI
Code: 328674(28)

Total Theory Periods: 40
No. of class Tests to be conducted: 2 (Minimum)
ESE Duration: Three Hours

Course objective:
1. To study the fabrication process of monolithic ICs.
2. To study the dielectric and magnetic property of materials.
3. To understand the characteristics of various components.

Course Outcome:
1. Student will be able to understand the fabrication process of Diodes and Transistors.
2. Student will be able to understand the properties of materials used in semiconductor devices.

UNIT I
Monolithic Techniques: The basic fabrication sequence; Growth and refining of silicon crystals; Epitaxial process; Diffusion; Diffusion system; Surface passivation; Photolithography; Metallization; Isolation; Crossovers. Monolithic Transistors and diodes; Monolithic junction FET and MOSFET; Integrated resistors; Junction Capacitors. MOS ICs; The silicon –gate and silicon-nitride MOS structure; Advantages and limitations of MOS devices; Charge coupled devices.

UNIT II
Dielectric Properties of Insulators: Static Field; static Dielectric Constant; Polarization; Dielectric Constant of Monatomic gases; Dielectric constant of solids. Properties of Ferro electric materials; Spontaneous polarization Piezo Electricity, Alternating fields; Electronic and Ionic Polarizability-Frequency Dependence; Complex Dielectric Constant of Non-Dipolar Solids; Dipolar Relaxation and Dielectric Losses.

UNIT III

UNIT IV
Conduction in Metals: Ohm’s Law; Relaxation; Collision Time and Mean Free Path; Electron Scattering and Receptivity of Metals; Heat Developed in Current Carrying Conductors; Thermal Conductivity of Metals.

UNIT V

Name of Text Books:
2. Electrical Engineering Materials – A.J. Dekker, PHI.

Name of Reference Books:
1. Integrated Electronics – Millmann & Halkias, TMH
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch: Electronics & Telecommunication Engineering  
Subject: Computer Organization & Architecture  
(Professional Elective – I)

Duration of the Programme: Four Years

Course objective:
1. To know about Central processor organization.
2. To know about Control unit organization.
3. To provide an Insight into Arithmetic processor design.
4. To provide an insight into Input/Output organization & Memory organization.

Course Outcome:
1. Student will be able to understand Central processor organization.
2. Student will be able to understand Instruction set and micro programming.
3. Student will be able to understand Algorithm in arithmetic control unit.
4. Student will be able to understand Input/output and memory organization.

UNIT I  **Central Processor organization:** Bus organized computer, Memory address structure, Memory data register, program counter, Accumulator, Instruction register, Program counter, Accumulator, Instruction register, Instruction field, Micro operations, Register transfer languages, Instruction field, Decoding and execution, Instruction formats and addressing modes.

UNIT II  **Control unit organization:** Instruction sequencing, Instruction interpretation, Hardwired control, Micro-programmed control organization, Control memory, Address sequencing, Micro-instruction, Formats, Micro-program sequence, Microprogramming.

UNIT III  **Arithmetic processor design:** Addition and subtractions algorithm, Multiplication algorithm, Division algorithm Processor configuration, Design of control unit and floating point arithmetic.

UNIT IV  **Input Output organization:** Programmed I/O, I/O addressing, I/O instruction, Synchronization, I/O interfacing, Interrupt mechanism, DMA, I/O processors and data communication, RISC, CISC, Loosely Coupled & Tights Coupled system.

UNIT V  **Memory organization and multiprocessing:** Basic concepts and terminology, Memory hierarchy, Semiconductor memories (RAM, ROM), Multiple module, Memories and interleaving (Virtual memory, Cache memory, Associative memory), Memory management hardware requirements, RISC & CISE Processor.

**Name of Text Books:**
1. Computer System Architecture by M. Morris Mano, PHI
2. Computer Organization Architecture by J.P. Hayes, PHI

**Name of Reference Books:**
1. Digital Computer Logic Design By M. Morris Mano, PHI
2. Structured Computer Organization by Andrew S. Tanenbaum PHI

Name of the Programme: Bachelor of Engineering  
Duration of the Programme: Four Years
Chhattisgarh Swami Vivekanand Technical University, Bhilai

Branch: Electronics & Telecommunication Engineering  
Subject: Advanced Semiconductor Devices  
(Professional Elective – I)

<table>
<thead>
<tr>
<th>Course objective:</th>
<th>Course Outcome:</th>
</tr>
</thead>
</table>
| 1. To study the concepts of metal Semiconductor devices.  
2. To understand concept of Tunnelling study tunnel devices.  
3. To introduce concept of Transferred electron effect and Study various modes of such devices.  
4. To study about advanced MOS Devices. | 1. Student will be able to understand concepts of MESFET, CCDS.  
2. Student will be able to understand concepts of tunneling .  
3. Student will be able to understand Transferred-Electron devices.  
4. Student gets an idea of MOSFET devices. |

UNIT I  **Metal Semiconductor Devices:** Metal-vacuum boundary: Schottky effect, Metal-Semiconductor boundary: Ohmic contact, Current transport across a metal-semiconductor boundary, Metal-Insulator-Semiconductor (MIS) System, Metal-Semiconductor-Field -Effect-Transistor (MESFET), Charge Coupled Devices (CCDs)

UNIT II  **Semiconductor Tunnel Devices:** Tunneling from the point of view of quantum measurement, Analysis of the Tunneling effect; Tunneling probability, Tunneling current density, Resonant tunneling. Tunnel Diodes; Qualitative and quantitative explanation of the Tunnel Diode I-V characteristics, Tunneling in a resonant tunneling diode, Indirect tunneling. Excess current, Thermal current in a tunnel diode, Dependence of tunnel diode characteristics on various parameters.


UNIT IV  **MOSFET:** Introduction, Basic Device Characteristics; Non-equilibrium condition, Linear and Saturation regions, Sub threshold region, Non-uniform Doping and Buried Channel Devices, Short-Channel Effects, MOSFET Structures; Scaled Down devices, HMOS, DMOS, Recessed-Channel MOSFET, Schottky-Barrier Source and Drain, Thin Film Transistor, SOI, VMOS, HEXFET.


**Name of Text Books:**
2. Physics of Semiconductor Devices, Michael Shur, PHI

**Name of Reference Books:**
2. Semiconductor Devices-Modelling & Technology, Nandita Dasgupta & Amitava Dasgupta, PHI

Name of the Programme: Bachelor of Engineering  
Duration of the Programme: Four Years