SSCET, BHILAI

Chhattisgarh Swami Vivekanand Technical University, Bhilai

SCHEME OF EXAMINATION

M.E. Electronics & Telecommunication (Specialization in VLSI Design)

THIRD SEMESTER

Sr. No.	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination Theory / Practical			Total Marks	Credit L+(T+P) / 2
				L	T	P	ESE	CT	TA		
1	Electronics & Telecom	560311 (28)	Analog VLSI	3	1	-	100	20	20	140	**4**
2	Refer Table- III		Elective - III	3	1	-	100	20	20	140	**4**
3	Electronics & Telecom	560321 (28)	Project	-	-	28	100	-	100	200	**14**
4	Electronics & Telecom	560322 (28)	Seminar on Industrial Training	-	-	3	-	-	20	20	**2**
TOTAL				**6**	**2**	**31**	**300**	**40**	**160**	**500**	**24**

Table- III

Elective-III			
Sr. No.	**Board of Study**	**Subject Code**	**Subject**
1	Electronics & Telecom	560331 (28)	Algorithm for VLSI Design Automation
2	Electronics & Telecom	560332 (28)	ASIC Design
3	Electronics & Telecom	560333 (28)	Design of Semiconductor Memories

L - Lecture T - Tutorial
P - Practical ESC – End Semester Exam
CT - Class Test TA – Teachers Assessment

Note (1) – **1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session.**

Note (2) – **Choice of elective course once made for an examination cannot be changed in future examinations.**

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Semester : **M. E. – III** Branch: **Electronics & Telecommunication**
Subject : **Analog VLSI**
Total Theory Periods : **40** Code: **560311(28**)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1

Basic current mirrors and single stage amplifiers – simple cmos current mirror – common source – common gate amplifier with current mirror active load – source flower with current mirror to supply bias current – high output impedance current mirrors and bipolar gain stages – frequency response.

UNIT 2
Operational amplifier design and compensation: two stage CMOS operational amplifier – feedback and operational amplifier compensation – advanced current mirrors – folded-cascode operational amplifier – current mirror operational amplifier – fully differential operational amplifier – common mode feedback circuits – current feedback operational amplifier. Comparator – charge injection error – latched comparators – BiCMOS comparators.

UNIT 3
Sample and hold and switched capacitor circuits : MOS, cMOS and biMOS sample and hold circuits – switched capacitor circuits – basic operation and analysis first order and biquad filters – charge injection – switched capacitor gain circuit – correlated double sampling techniques – other switched capacitor circuits.

UNIT 4
Data converters : ideal d/a and a/d converters – quantization noise – performance limitations. nyquist rate d/a converters – decoder based converters – binary scaled converters – hybrid converters. nyquist rate a/d converters – integrating – successive approximation – cyclic flash type – two step interpolating – folding and pipelined – a/d converters.

UNIT 5
Over sampling converters and filters : over sampling with and without noise haping – digital decimation filter – high order modulators – band pass over sampling converters – practical considerations – continuous time filters – mixers – PLLs - multipliers.

References

1. D.A. John and Ken Martin , “analog integrated circuit design” , John Wiley, 1st Edition, 1996.

2. Mohamed Ismail, “Analog VLSI” , Mc Graw hill, 1st Edition, 1994.

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Semester: **M. E. – III** Branch: **Electronics & Telecommunication**
Subject: **Algorithm for VLSI Design Automation**
Total Theory Periods: **40** Code: **560331 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Logic synthesis & verification
Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

UNIT 2
VLSI automation Algorithms: **Partitioning:** problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms. **Placement, floor planning & pin assignment**: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor plannning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

UNIT 3
Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

UNIT 4
Detailed routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms.

UNIT 5
Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization. **Compaction:** problem formulation, one-dimensional compaction, two dimension-based compaction, hierarchical compaction

Text:

1. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.
2. Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

References:

1. Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.
2. Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition

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Semester: **M. E. –III**
Branch: **Electronics & Telecommunication**
Subject: **ASIC Design**
Total Theory Periods: **40**
Code: **560332 (28)**
Total Marks in End Semester Examination: **100**
Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Introduction to ASICS, CMOS Logic and ASIC Library Design: Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort - Library cell design - Library architecture .

UNIT 2
Programmable ASICS, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells: Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT 3
Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry: Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools - EDIF- CFI design representation.

UNIT 4
Logic Synthesis, Simulation and Testing: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT 5
ASIC Construction, Floor Planning , Placement and Routing: System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

Text Book:

1. M.J.S .Smith, - " Application - Specific Integrated Circuits " - Addison -Wesley Longman Inc., 1997.

References:

1. Andrew Brown, - " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991.
2. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays " - Kluever Academic Publishers, 1992.
3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
4. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

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Semester: **M. E. – III** Branch: **Electronics & Telecommunication**
Subject: **Design of Semiconductor Memories**
Total Theory Periods: **36** Code: 560333 (28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Random Access Memory Technologies: Static Random Access Memories (SRAMs): SRAM cell structure- MOS SRAM architecture – MOS SRAM cell and peripheral circuit operation – bipolar SRAM technologies – silicon on insulator (SOI) technology – advanced SRAM architectures and technologies, application specific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM technology development – CMOS CRAMs – DRAMs cell theory and advanced cell structures- BiCMOS DRAMs-soft error failure in DRAMs – Advanced DRAM designs and architecture – application specific DRAMs.

UNIT 2
Nonvolatile Memories: Masked Read – only memories (ROMs): High density ROMs – programmable read-only memories (PROMs)- bipolar PROMs – CMOS PROMs – erasable (UV)- Programmble read-only memories (EPROMs)- Floating Gate EPROM cell- one – time progammable (OTP) Eproms – Electrically Erasable PROMs (EEPROMs) – EEPROM technology and architecture –nonvolatile SRAM-Flash memories (EPROMs or EEPROM) – Advanced flash memory architecture.

UNIT 3
Memory Fault Modeling, Testing and Memory Design for Testability and Fault Tolerance, RAM fault modeling, electrical testing, Peusdo random testing – megabit DRAM testing – nonvolatile memory modeling and testing – IDDQ fault modeling and testing – application specific memory testing.

UNIT 4
Semiconductor Memory Reliability and Radiation Effects: General Reliability issues – RAM failure modes and mechanism – nonvolatile memory reliability – reliability modeling and failure rate prediction – design for reliability – reliability test structures – reliability screening and qualification. Radiation effects – single event phenomenon (SEP)- radiation hardening techniques – radiation hardening process and design issues – radiation hardened memory characteristics – radiation hardness assurance and testing – radiation dosimetry – water level radiation testing and test structures.

UNIT 5
Advanced Memory Technologies and High-density Memory Packaging Technologies: Ferroelectric Random Access Memories (FRAMs) – Gallium Arsenide (GaAs) FRAMs – Analog memories magnetoresistive random access memories (MRAMs) – Experimental memory devices. Memory hybrids and MCMs (2D) – Memory stacks and MCMs (3D) – Memory MCM testing and reliability issues- memory cards- high density memory packaging future directions.

Books:

1. Ashok K.Sharma, “Semiconductor Memories Technology, Testing and Reliability”, Prentice hall of India Private Limited, New Delhi 1997.