SSCET, BHILAI

Chhattisgarh Swami Vivekanand Technical University, Bhilai

SCHEME OF EXAMINATION

M.E. Electronics & Telecommunication (Specialization in VLSI Design)

SECOND SEMESTER

Sr. No.	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination			Total Marks	Credit L+(T+P) / 2
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1	Electronics & Telecom	560211 (28)	Digital Logic with Verilog Design	3	1	-	100	20	20	140	**4**
2	Electronics & Telecom	560212 (28)	VLSI System Testing	3	1	-	100	20	20	140	**4**
3	Electronics & Telecom	560213 (28)	Low Power VLSI Design	3	1	-	100	20	20	140	**4**
4	Electronics & Telecom	560214 (28)	Embedded System Design	3	1	-	100	20	20	140	**4**
5	Refer Table II		Elective – II	3	1	-	100	20	20	140	**4**
6	Electronics & Telecom	560221 (28)	Verilog Design and verification Lab	-	-	3	75	-	75	150	**2**
7	Electronics & Telecom	560222 (28)	Embedded system Lab	-	-	3	75	-	75	150	**2**
TOTAL				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

Table- II

Elective- II			
Sr. No.	**Board of Study**	**Subject Code**	**Subject**
1	Electronics & Telecom	560231 (28)	MEMS and IC integration
2	Electronics & Telecom	560232 (28)	MOS Physics
3	Electronics & Telecom	560233 (28)	Neural Network for VLSI

L - Lecture T - Tutorial
P - Practical ESC – End Semester Exam
CT - Class Test TA – Teachers Assessment

Note (1) – 1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session.

Note (2) – Choice of elective course once made for an examination cannot be changed in future examinations.

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Semester: **M. E. – II** Branch: **Electronics & Telecommunication**
Subject: **Digital Logic with Verilog Design**
Total Theory Periods: **40** Code: **560211 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Introduction to logic circuits: Variables and functions, Sysnthesis using AND, OR and NOT gates, Introduction to CAD tools, Introduction to Verilog

UNIT 2
Implementation Technology: Transistor switches, CMOS Logic, PLD, Transmission gates

UNIT 3
Optimized Implementation of Logic Functions: Strategy for minimization , minimzation of POS, Multiple Output circuits, Analysis of Multilevel Circuits

UNIT 4
Number Representation and Arithmetic Circuits: Positional Number representation, Addition of unsigned numbers, signed Numbers, Fast adders, Design of arithmetic circuits using CAD tools, Multiplication

UNIT 5
Combinational Circuit Building blocks: Multiplexers, Decoder, Encoder, Code Converters, Arithmetic Comparison circuits, Verilog for combinational circuits
Design of Sequential design, Design Asynchronous Sequential Design

Text:

1. Fundamental of digital Logic with Verilog design by S. Brown & Z. Vransesic, TMH.
2. Verilog primer by J.Bhasker , Pearson education

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject : **VLSI System Testing**
Total Theory Periods : **40** Code: **560212 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods : **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Special purpose Subsystems: Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc.
Design Economics: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Personpower, example

UNIT 2
TESTING OF COMBINATIONAL CIRCUITS: Faults in digital circuits – Failures and faults – Modeling of faults – Temporary faults – Test generation for Combinational logic circuits – testable combinational logic circuit design – Scan based design and JTAG testing issues.

UNIT 3
TESTING OF SEQUENTIAL CIRCUITS: Test generation for sequential circuits – Design of testable sequential CK5- Built in self test – Testable memory design.

UNIT 4
VERIFICATION AND TESTING: Verification – Timing verification – Testing concepts – Fault coverage – ATPG – Types of tests – Testing FPGAs – Design for testability.

UNIT 5
VLSI System Testing & Verification: Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan.
VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.

Text:

1. Neil H.E. Weste, Davir Harris, “CMOS VLSI Design: A Circuits and system perspectives” Pearson Education 3rd Edition.
2. Wayne, Walf, “Modern VLSI design: System on Silicon” Pearson Education, Second Edition

References:

1. Pucknull, “Basic VLSI Design” PHI 3rd Edition

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject : **Low Power VLSI Design**
Total Theory Periods : **40** Code: **560213 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods : **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1

Need for l+ow power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT 2

Power estimation

Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation.

Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT 3

Low Power Design

Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level:

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

UNIT 4

Low power Architecture & Systems:

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT 5

Low power Clock Distribution : Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & architectural level methodologies : Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

References:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject : **Embedded System Design**
Total Theory Periods: **40** Code: **560214 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT I

REVIEW OF EMBEDDED HARDWARE: Terminology Gates - Timing Diagram - Memory - microprocessors Buses-Direct Memory Access-interrupts - Built-ins on the Microprocessor-Conventions Used on Schematic-schematic. Interrupts Microprocessor Architecture-Interrupt Basics-Shared Data Problem-Interrupt latency.

UNIT 2

PIC MICROCONTROLLER AND INTERFACING: Introduction, CPU architecture, registers, instruction sets addressing modes Loop timing, timers, Interrupts, Interrupt timing, I/o Expansion, I 2C Bus Operation Serial EEPROM, Analog to digital converter, UART-Baud Rate-Data Handling-Initialisation, Special Features - serial Programming-Parallel Slave Port.

UNIT 3:

EMBEDDED MICROCOMPUTER SYSTEMS: Motorola MC68H11 Family Architecture Registers, Addressing modes Programs. Interfacing methods parallel I/O interface, Parallel Port interfaces, Memory Interfacing, High Speed I/o Interfacing, Interrupts-interrupt service routine-features of interrupts-Interrupt vector and Priority, timing generation and measurements, Input capture, Output compare, Frequency Measurement, Serial I/o devices Rs.232, Rs.485. Analog Interfacing, Applications.

UNIT 4

SOFTWARE DEVELOPMENT AND TOOLS: Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Intergrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators.

UNIT 5

REAL TIME OPERATING SYSTEMS: Task and Task States, tasks and data, semaphores and shared Data Operating system Services-Message queues-Timer Function-Events-Memory Management, Interrupt Routines in an RTOS environment, basic design Using RTOS.

Text Books:

1. David E Simon, " An embedded software primer ", Pearson education Asia, 2001.
2. John B Peat man " Design with Microcontroller ", Pearson education Asia, 1998.
3. Jonartthan W. Valvano Brooks/cole " Embedded Micro computer Systems. Real time Interfacing ", Thomson learning 2001.

References:

1. Burns, Alan and Wellings, Andy, " Real-Time Systems and Programming Languages ", Second Edition. Harlow: Addison-Wesley-Longman, 1997.
2. Raymond J.A. Bhur and Donald L.Bialey, " An Introduction to real time systems: Design to networking with C/C++ ", Prentice Hall Inc. New Jersey, 1999.
3. Grehan Moore, and Cyliax, " Real time Programming: A guide to 32 Bit Embedded Development. Reading " Addison-Wesley-Longman, 1998.
4. Heath, Steve, " Embedded Systems Design ", Newnes 1997.

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject : **MEMS and IC Integration**
Total Theory Periods: **40** Code: **560231 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Introduction, Evolution of Microsensors and MEMS, micrometallurgy and material characterization, microscopy and visualization, lateral and vertical dimensions, electrical measurements, physical and chemical analysis, XRD, TXRF, SIMS, AES, XPS, RBS, EMPA, analysis area and depth

UNIT 2
Silicon material properties, crystal growth, crystal structure, wafer process, Thin Film Material and Process: PVD and CVD, Metallic thin films and Dielectric thin films, properties of dielectric film, Epitaxy, Thin Film Growth and Structure: PVD and CVD film growth and structure.

UNIT 3
Pattern generation, optical lithography, lithographic patterns, etching: wet etching, electromechanical etching, anistropic wet etching, plasma etching, wafer cleaning and surface preparation.

UNIT 4
Microstereolithography for MEMS: Photopolymorization, stereolithographic system, microstereolithography, scanning methods, two photon MSL, other MSL approaches, Polymeric MEMS architecture with silicon, metal and ceramics, combined structure and applications RF MEMS, and Optical MEMS

UNIT 5
Microsensors: Thermal sensors, Radiation Sensors, magnetic sensors, Biochemical sensors,Indroduction to SAW Devices, MEMS-IDT Microsensors: Principle, fabrication, testing wireless readout, hybrid accerolometers and gyroscope.

Text:

1. Introduction to Microfabrication, Sami Franssila, John Wiley,
2. Microsensors MEMS and Smart Devices, Gardner, John wiley

Refrences:

1. Masood Tabib-Azar, Microactuators, Kluwer, 1998.
2. Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994
3. D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997

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Semester: **M. E. – II** Branch: **Electronics & Telecommunication**
Subject: **MOS Physics**
Total Theory Periods: **40** Code: **560232 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
MOS Device Physics: Triode Region, Saturation Region, Avalanche Region, Sub threshold Region, Second Order Effects, Ways of Measuring Threshold Voltage, MOS Device Applications.

UNIT 2
Small-Geometry Effects: Nonuniform doping & Effect on Threshold voltage, Sub tThreshold current, Short-channel effect, Narrow width effect, Small-Geometry effects, Shrink & Scaling, Scaling down the Dimensions of MOS Devices.

UNIT 3
MOS IC Processes: Metal Gate PMOS, The Hypothetical Metal-Gate NMOS, Metal-Gate CMOS, Silicon Gate LOCOS NMOS Processes, The HMOS Process, Process Enhancements.

UNIT 4
MOS Digital IC Design: Building Blocks for MOS digital IC, Inverter DC Analysis, Inverter Transient Analysis, MOS Logic Circuits, Memory Circuits, Other Circuit Techniques.

UNIT 5
Analog MOS Design: Considerations in Analog MOS circuits, Analog Building Blcoks, MOS Operational Amplifiers, Capcitor Based Circuits, Switched Capacitor Filters, Charge Coupled Devices, Charge Coupled Device Applications

Text:

1. DeWitt G. Ong "Modern MOS Technolgy: Processes, Devices and Design" McGraw Hill Book Co.
2. Charels P. Pfleeger "Security in Computing" Prentice Hall

References:

1. Jeff Crume "Inside Internet Security" Addison Wesley

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject: **Neural Network for VLSI**
Total Theory Periods: **40** Code: **560233 (28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1
Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons

UNIT 2
ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning.

UNIT 3
Supervised Learning and Neurodynamics: Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

UNIT 4
Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ART networks, LVQ

UNIT 5
Applications for VLSI Design: Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Text:

1. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999
2. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International,
   New Jersey, 1999.

Reference:

1. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques", Addison-Wesley, Reading, Mass, (1992).
2. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.
3. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject : **Verilog Design and Verification Lab**
Total Practical Periods : **40** Code: **560221 (28)**

Total Marks in End Semester Examination: **75**

List of experiments to be performed:

1. 8 bit shift register
2. 8:1 multiplexer
3. Barrel shifter
4. N by m binary multiplier
5. RISC CPU (3bit opcode, 5bit address)
6. SPICE simulation of basic analog circuits.
7. Verification of layouts (DRC, LVS)

Tools used : Cadence tools, Mentor Graphics tools, lab view tools, multisim, SILVACO

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Semester : **M. E. – II** Branch: **Electronics & Telecommunication**
Subject : **Embedded System Lab**
Total Theory Periods : **40** Code: **560222 (28)**

Total Marks in End Semester Examination: **75**

List of experiments to be performed:

(i) Create ,compile and test a program to print a string a message on standard output device
(ii) Create a program to print powers of 2 from 2^0 to 2^{12}
(iii) Write a program tht continuously reads Port A and provides output to port B
(iv) Use External Hard ware Interrupt to print a message to the standard output devices each time an interrupt occurs . Also print number of time interrupt occur
(v) Create a program that will turn on an LED when falling edge occur on external interrupt 0 and turn it off when rising edge occour on external interrupt 1
(vi) Create a programme that will demonstrate how watchdog timer resets the processor if programme hangs up to infinite loop
(vii) Create a programme that will read the data on all 8 bits of port B swap the nibble of data and send it to port A
(viii) Create a simulated engine speed monitor that will light a LED if the motor speed drops below 200rpm and another LED if motor speed exceed 500 rpm and light another LED if motor speed between 200 to 500 rpm
(ix) Create a programme to output the ASCII character G every 50 msec via USART at 9600 baud rate
(x) Write a microcontroller 8051 program to add two floating-point numbers.
(xi) Write a microcontroller 8051 program to multiply two floating-point numbers.
(xii) Write a microcontroller 8051 program that generates 2kHz square wave on pin P1.0, 2.5 kHz on pin P1.2 and 25 Hz on pin P1.3.
(xiii) Write a microcontroller 8051 program for counter 1 in mode 2 to count the pulses and display the state o the TL1 count on P2. Assume that the clock pulses are fed to pin T1.
(xiv) Write a microcontroller 8051 program to transfer word “COMMUNICATION” serially at 4800 baud and one stop bit, to the com port of PC continuously.
(xv) Write a microcontroller 8051 program to receive bytes of data serially, and put them in P1. Set the baud rate at 2400 baud, 8-bit data, and 1 stop bit. Assume crystal frequency to be 11.0592 MHz.

Recommended Books:

1. Embedded C Programming and the Microchip by PIC Barneet , Cox ,O’cull Thomson publication
2 Embedded system by Raj Kamal TMH

List of Equipments/Machine Required :

1. MATLAB Software with Simulink
2. Emulation software with Cross C complier