

Chhattisgarh Swami Vivekanand Technical University, Bilai

SCHEME OF EXAMINATION

M.E. Electronics & Telecommunication (Specialization in VLSI Design)

FIRST SEMESTER

Sr No	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination			Total Marks	Credit L+(T+P) /2
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1	Electronics & Telecom	560111 (28)	VLSI Technology	3	1	-	100	20	20	140	4
2	Electronics & Telecom	560112 (28)	VLSI System Design	3	1	-	100	20	20	140	4
3	Electronics & Telecom	560113 (28)	MOS Circuit Design	3	1	-	100	20	20	140	4
4	Electronics & Telecom	560114 (28)	Modelling with HDLs	3	1	-	100	20	20	140	4
5	Refer Table 1		Elective – I	3	1	-	100	20	20	140	4
6	Electronics & Telecom	560121 (28)	VHDL Modelling Laboratory	-	-	3	75	-	75	150	2
7	Electronics & Telecom	560122 (28)	Computer Simulation Laboratory	-	-	3	75	-	75	150	2
TOTAL				15	5	6	650	100	250	1000	24

Table-I

Elective-I			
Sr. No.	Board of Study	Subject Code	Subject
1	Electronics & Telecom	560131 (28)	CMOS RF Circuit Design
2	Electronics & Telecom	560132 (28)	Real Time System & Software
3	Electronics & Telecom	560133 (28)	Digital Image Processing

L - Lecture
P - Practical
CT - Class Test

T - Tutorial
ESC – End Semester Exam
TA – Teachers Assessment

Note (1) – 1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session .

Note (2) – Choice of elective course once made for an examination cannot be changed in future examinations.

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SECOND SEMESTER

Sr · No.	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination			Total Marks	Credit L+(T+P) / 2
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1	Electronics & Telecom	560211 (28)	Digital Logic with Verilog Design	3	1	-	100	20	20	140	4
2	Electronics & Telecom	560212 (28)	VLSI System Testing	3	1	-	100	20	20	140	4
3	Electronics & Telecom	560213 (28)	Low Power VLSI Design	3	1	-	100	20	20	140	4
4	Electronics & Telecom	560214 (28)	Embedded System Design	3	1	-	100	20	20	140	4
5	Refer Table II		Elective – II	3	1	-	100	20	20	140	4
6	Electronics & Telecom	560221 (28)	Verilog Design and verification Lab	-	-	3	75	-	75	150	2
7	Electronics & Telecom	560222 (28)	Embedded system Lab	-	-	3	75	-	75	150	2
TOTAL				15	5	6	650	100	250	1000	24

Table- II

Elective- II			
Sr. No.	Board of Study	Subject Code	Subject
1	Electronics & Telecom	560231 (28)	MEMS and IC integration
2	Electronics & Telecom	560232 (28)	MOS Physics
3	Electronics & Telecom	560233 (28)	Neural Network for VLSI

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P - Practical
CT - Class Test

T - Tutorial
ESC – End Semester Exam
TA – Teachers Assessment

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THIRD SEMESTER

Sr. No.	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination			Total Marks	Credit L+(T+P) / 2
				L	T	P	Theory / Practical				
							ESE	CT	TA		
1	Electronics & Telecom	560311 (28)	Analog VLSI	3	1	-	100	20	20	140	4
2	Refer Table- III		Elective - III	3	1	-	100	20	20	140	4
3	Electronics & Telecom	560321 (28)	Project	-	-	28	100	-	100	200	14
4	Electronics & Telecom	560322 (28)	Seminar on Industrial Training	-	-	3	-	-	20	20	2
TOTAL				6	2	31	300	40	160	500	24

Table- III

Elective-III			
Sr. No.	Board of Study	Subject Code	Subject
1	Electronics & Telecom	560331 (28)	Algorithm for VLSI Design Automation
2	Electronics & Telecom	560332 (28)	ASIC Design
3	Electronics & Telecom	560333 (28)	Design of Semiconductor Memories

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FOURTH SEMESTER

Sr. No.	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination			Total Marks	Credit L+(T+P)/2
							Theory / Practical				
				L	T	P	ESE	CT	TA		
1	Electronics & Telecom	560421 (28)	Project + Seminar on Project	6	-	34	300	-	200	500	23
TOTAL				6	-	34	300	-	200	500	23

L - Lecture
P - Practical
CT - Class Test

T - Tutorial
ESC – End Semester Exam
TA – Teachers Assessment

Scheme of Marks Allotment

Semester	Total Marks	Grand Total
I	1000	3000
II	1000	
III	500	
IV	500	